To Whom It May Concern:

Date September 17, 2009

On JULY 13, 2009 at 1:00 PM I gave a lecture on "How can we solve a problem physically on an assembly of organic molecule: A journey towards realizing a practical "nano-brain" at the TecEdge: 5100 Springfield Pike, Suite 210 Dayton, OH 45431 The talk was organized by Dr. Saber Hussain at 937- 904-9517 and Dr Ewing Robert (RYRT) 937-255-6427 x4216.

About 25-30 people attended the lecture. Some of these included Dr Robert Ewing, Chrissy Grabinski, Nikki Schaeublin, Dr Laura Stolle, Carol Garrett, David Ellis, Janice Speshock, Amanda Schrand, Michael Moulton, Kali Spears, Beth Maurer, Monita Sharma, Marcus Smith, Karl Strieker, Dr Nancy Kelley-Loughnane. The lecture was followed by an interesting question and answer (Q and A) session.

After Q and A session Dr. Saber arranged a meeting on how can we formulate the visit into an effective future collaboration. We had an hour-long discussion where every single member of the close associates of Dr. Saber described their work in details and then we found the route towards it. We envisioned how the information-processing capabilities of a single cell could be used for a variety of bloodless medical procedures. To that end, and to satisfy the requirement for a state of the art review, I have appended a Japanese patent I have filed in this area.

This is very well regarded that the intelligence of a single cell, information-processing and communication is controlled by bundles of microtubules. One of the fundamental aspects of future nano-robots to carry out bloodless, fatal less medical surgery is to understand the fundamentals of this information processing so that it does not destroy the entire system rather than saving it from degradation. Therefore, revealing the mysterious electronics and communication properties of microtubules is to be resolved prior to bringing such medical surgery into practice. In this regard, we strongly believed that microtubule study and toxicology investigation are two prime parts of "nano-brain" studies. Thus, the Dayton trip ended in a success.

Dr. Anirban Bandyopadhyay
Advanced Scanning Probe Microscopy Group
Advanced Nano Characterisation Center
National Institute for Materials Science
1-2-1 Sengen, Main Bldg, Room-815
Tsukuba, Ibaraki, Japan
Tele-0081-29-859-2167 office
0081-29-859-2801 FAX

Official Homepage http://www.anirbanlab.co.nr

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14. ABSTRACT
It is very well regarded that the intelligence of a single cell, information-processing and communication is controlled by bundles of microtubules. One of the fundamental aspects of future nano-robots to carry out bloodless, fatal less medical surgery is to understand the fundamentals of this information processing so that it does not destroy the entire system rather than saving it from degradation. Therefore, revealing the mysterious electronics and communication properties of microtubules is to be resolved prior to bringing such medical surgery into practice. In this regard, we strongly believed that microtubule study and toxicology investigation. This report is mainly comprised of a Japanese patent I filed, dealing with new vertical parallel processor(or referred to simply ?a vertical processor?) following working principle of neural network, a modified virtual source neural network model which comprises the above vertical parallel processor, and a processor training method to train single vertical parallel processor of the above vertical parallel processor. These principles will be utilized in developing new Air Force-sponsored protocols geared toward understanding how the human cell uses microtubules for information processing.

15. SUBJECT TERMS

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[Title of Invention]

Vertical parallel processor

[Field of the Invention]

[0001]

This invention relates to a new vertical parallel processor(or referred to simply “a vertical processor”) following working principle of neural network, a modified virtual source neural network model which comprises the above vertical parallel processor, and a processor training method to train single vertical parallel processor of the above vertical parallel processor.

[Background of the Invention]

[0002]

In any sequential processor each bit is processed one by one, even if the processor is a teraflop one. But in brain process thousands of bits is processed at a time even if it is slow. There has been several models developed to copy neural system via software and many experimental set up have been proposed copying the property of neural activities. For an example creating ion channels [patent ref. 1] and introducing threshold potential in response to make a neural modeling device. Neurons have been designed using capacitor and floating gate transistor [patent ref. 2] and analyzed with equivalent neural network models. Physical neural network with multiple signal input and output to strengthen or weaken connectivity is also realized [patent ref. 3]. Apart from designing neurons many models have been developed to analyze random network. But none of the model could propose a set up that could really allow copying the basic features of neural system in solid-state device.

[0003]

The neural system following these models uses electronic components which generate substantial heat during information processing, thus cannot be minimized at nanoscale dimension. Introduction of molecular electronics addressed the basic issues of nanoscale computation via generating concept of multilayer perceptron [patent ref. 4] with DNA oligomers or generating random path on a processing surface through switching molecules [patent ref. 5]. Most of these random neural networks learn to operate via constructing a decision function [patent ref. 6] mostly applying the working principle of our brain [patent ref. 7]. Though there have been several proposal for intelligent control of machines [patent ref. 8] basic issues of signal transport from one neuron to another eventually is developing a sequential connection which is destroyed with failure of any system unit. There are some projects, which somehow try to overcome the sequentiality by fuzzy logic but compromising the contribution of individual to the final output. One such example is the project nanocell [non-patent ref. 5]

[0004]

Problems of integrating molecules into a physical chip are overcome in the development of Nanocell [non-patent ref. 2-4] by teaching overall response of randomly oriented switches as a behavior of logic gate say a NAND gate. Major change in Nanocell than other model was avoidance of wiring of single molecule, which is conformational change sensitive, hence could not be reliable in integrated circuit. So challenge of critical dimension was penetrated by intelligent logication of a fuzzy system. Similar to

Nanocell there are many model developed till date for logication of fuzzy system though several neural modeling devices and instruments operating on ANN logic have been designed. Nanocell is different only in sense that it proposed alternative way of addressing molecular electronics in processor.

[0005]

Though Nanocell is realized but it has several limitations apart from dimensional requirement. As input and output is taken on the same surface at two different ends if a particular region stops working the whole logic pattern changes. It is sensitive to noise. Change in an array of inputs is only entertained if it significantly changes the final output. And it may be possible that for different array we end up with same output. Number of outputs and number of inputs are complementary to each other in a fixed operational area. If the number of input increases number of output will decrease. Switches work at random in an absolute unpredictable way and role of individual smart system or switches or neuron is neither taken into account nor is it necessary. In nanocell we are interested only in final changes of output current; it does not matter whether different input flows current through different path and finally result in the same output. So physically the interplaying surface is a black box that provides different set of current output for different set of input voltages. It could be modeled as array of electrodes with randomly connected non-linear electronic components. Switches and paths are generators of non-linearity.

As applications of nanocells are nowadays realized or proposed in different modes and systems [non-patent ref. 6], we call all similar systems as Nanocell systems.

[0006]

[patent ref. 1] U.S. 5,378,342
[patent ref. 2] U.S. 5,343,555
[patent ref. 3] U.S. 6,889,216 B2
[patent ref. 4] U.S. 6,741,956 B1
[patent ref. 5] U.S. 6,820,244 B2
[patent ref. 6] U.S. 6,886,008 B2
[patent ref. 7] U.S. 4,954,963
[patent ref. 8] U.S. 6,882,992 B1

[0007]

[non-patent ref. 1] J. Hopfield, Neural networks and physical systems with emergent collective computational abilities, 79 Proc. Natl. Acad. of Sci. USA 2554 (1982).
[non-patent ref. 2] Summer M. Husband, Programming in Nanocell a random array of molecules, Rice University PhD thesis April 2002 available at http://www.caam.rice.edu/caam/trs/2002/TR02-04.pdf
[non-patent ref. 3] Christopher P. Husband, Summer M. Husband, Jonathan S. Daniels, and James M. Tour, Logic and Memory With Nanocell Circuits, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 9, SEPTEMBER 2003 pp-1865
[non-patent ref. 4] James M. Tour, William L. Van Zandt, Christopher P. Husband, Summer M. Husband, Lauren S. Wilson, Paul D. Franzon, and David P. Nackashi, Nanocell Logic Gates for Molecular Computing, IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 1, NO. 2, JUNE 2002 pp-100
[non-patent ref. 5] Nanocell project proposal, available at http://www.eng.yale.edu/reedlab/protected/proposals/nanocell-full-proposal.pdf

[non-patent ref. 6] N. J. Wu, H. Lee, Y. Amemiya, H. Yasunaga, Methods for determining weight co-efficients for Quantum Boltzman Machine neuron devices, Jpn JAP, 38, 439 (1999)
[non-patent ref. 7] Supriyo Datta, Magnus Paulsson, Ferdows Zahid, Electrical Conduction through Molecules, available at http://www.nanohub.org/com_docman/task,down/bid,84/

[Disclosure of Invention]
[Purpose of Invention]
[0008]

The purpose of this invention is to develop a realistic neural model(set of trick or rules) and a device (processor) in principle, which can operate, based on the working principle of brain considering the proposed neural model. Such a principle based devices could have large industrial application as data processing is much faster, reliability is more, versatile as it is based on multilevel processing of information, flexible to modify with system requirement. Processing of completely different kind of information and taking decision simultaneously was unknown till now. There existed no model or device in principle or realistic which can process more than 1 bit at a time in a single unit (supercomputer have several parallel such unit), no model could survive decision making under noise and death of basic elements like brain. Our final purpose is to provide all these features in a single processing system.

[Summary of Invention]
[0009] (★corresponding to Claim 1)

The inventors of this inventon conceived 3D multibit vertical parallel processor based on principles of neuron's collective computation in a brain, and completed this invention. Namely, this invention relates to the following vertical parallel processor, cluster having the above vertical parallel processor, modified virtual source neural network model and processor training method, using the said vertical parallel processor or cluster.

Firstly, this invention provides **a vertical parallel processor (also named "normal vertical parallel processor") comprising a coupled template, wherein plural input signals are given horizontally from all directions on a surface situated in the middle of surrounding electrodes where the surface contains multilevel systems or neurons and output signals are taken vertically at different points on that surface.**

In this specification, we call this processor "vertical parallel processor" or simply "vertical processor", as input and output are perpendicular to each other(see Fig.1, Fig.6). The surface of template on which multilevel systems sit is called processing surface. And a system that shows multilevel conductivity i.e. more than one conductivity at a particular bias is called multilevel system or neuron.

[0010] (★corresponding to Claim 13)

Secondly, this invention provides **a cluster (see Fig. 18) which comprises the above (normal) vertical parallel processors;**
neural node controller; and
connections motors sensors connected following ways A, B and C.

A. Some or all of the processors input connected to an array of vertical processors, rest of them to output of sensors which are free input of the whole system;

B. Some of its output connected to some of the output motors and rest of them connected to other vertical processors;

C. All free outputs connected to motors and not connected to any input of the whole system, taken vertically as a final cluster output.

Here, "cluster" means a system consisting of a few number of processors, neural node controller, connections, motors, and input signal converter array.

[0011] (★corresponding to Claim 14)

Thirdly, this invention provides **a modified virtual source neural network model (see Fig. 11) which comprises any one of the above vertical parallel processor, and its modification contains all of the following A, B and C.**

A. Binary neuron (having value 0 or 1) or continuum neurons (any value 0 to 1) of old concepts is replaced by multilevel system or neurons (selected values between 0 to 1).

B. Introduction of virtual sources as effective input to each neuron does not come from other neurons.

C. Modification is accession to individual outputs as we take output vertically; hence model becomes a 3D (3 dimensional) model.

This invented virtual source neural network model has been developed from Hopfield principle of 1982 (Fig. 11) to fit with the above vertical parallel processor. Here, "model" means a set of basic principle, trick or rules to be followed during development of training software for real time operations.

[0012] (★corresponding to Claim 17)

Forthly, this invention provides **a processor training method (see Fig. 12) to train single vertical parallel processor of the above invented vertical parallel processor, where input and output are correlated by the above invented artificial neural network model finding rule or weight coefficients of virtual neurons or multilevel systems following major initialization of the below training steps (1)-(3).**

(1) Firstly finding range of application (see Fig. 13) for local bias and global bias;

(2) secondly finding their levels of operations or functional behavior for each multilevel logic states (see Fig. 13);

(3) finally developing (or finding) logical function by energy minimization so that when an unpredictable input is given it can give most probable solution of the problem (Fig. 14).

[Advantageous effects]

[0013]

(Comparison with present processors)

It was suggested in U.S. patent 6,820,244 B2 which describe training of nanocell that vertical observation on the interplaying surface is impractical to use for large scale.

But if we can consider the vertical electrode array system as an integral part of whole neural network we can turn disadvantage into smarter system in many respects. Going vertical not only changes the basic design but changes the basic working principle completely from the established concepts of Nanocell like processors. Then, on the horizontal surface we have only different inputs coming from all directions and all

outputs are taken vertically. Each vertical electrode is a neural network output, and processes data parallely as signal processing through surface paths is not required as in sequential processors like nanocell processors. Performance also expected to be extremely fast as only few multilevel units are required to switch for one output point almost independent of each other.

[0014]

In our system the interplaying surface is not a black box anymore as now we can see and understand how we get output and how much it differs from expectation and how it differs. Electric field, potential and potential gradient at every point on interplaying surface is known; which sets smart systems into multilevel states, which could be predicted, as we know the states energetically. Unlike nanocell and like brain vertical output is a surface with hills and dips of current. And if some of the smart systems on the surface do not switch that won't change the position of hills and dips so there will be no effect on the solution. Simple problems of nanocell like processors whether any input shall have any effect in solution does not arise any more. It copies extremely parallel neural processors like our brain in many senses. ANN is used to find rule that the device follows to evolute different surfaces at different array of inputs. Where "nanocell" trains input and output signals to behave as a logic gate, we do not need the logic gate as our vertical processor can be an interface between natural world through sensor arrays and organs where multiple motors need multilevel control to operate properly.

[0015]

We summarize all these advantageous changes below.

1. This invention model device is simple but added new features than Hopfield model of neural network and capable of realization experimentally without compromising information processing advantages of neural systems of our brain. For an example it does not need logic gate.

2. The invention model is flexible to materials used, dimensional constraint of operational area be used in complex integrated circuit in principle without destroying its basic working parameters.

3. This invention is the only system that process more than one bit at a time hence could be operational with extreme parallel bit processing. This is truly parallel processor. A 1cm^2 processing surface can process 1 terabit (10^{12} bit) simultaneously if there are 1 switch/100nm^2 area; whereas any processor in the world process only 1 bit at a time. This means if each switch operate at 1GHz then it can process data $10^{12}\times10^{9}=10^{21}$ bits/sec!!

4. This invention is the only model proposed where decision survives even under extreme noise like our brain as decision making depends on response at significant co-ordinates not on contribution of everybody.

5. This invention can lead us towards serious developing of hardware capable of matching human brain as fuzzy integrated circuit developed by connecting our processors by random interconnection can also generate logic following vertical projection concept we introduced.

6. This invention model could experimentally realize collective computation (e.g. looking, thinking, working) without compromising the principle; this is only neural model that can take into account every significant contributor of decision-making unit.

7. This invention model is flexible towards materials used, addressing different functionality simultaneously, dimensionality of processing surface or number of electrodes used and no connectivity constraints.

8. This invention model can develop extreme sensor device, which can generate 3D pattern of the sensing parameter.

9. This invention model is flexible towards operation of mathematical functions as we can use it both way, horizontal-vertical and vertical-horizontal modes.

10. This invention model is the only existing model that survives its decision even some of its processing unit (neurons) fail to perform on the processing surface.

[Detailed Description of Invention]

[0016]

Next we explain this invention in detail.

[0017] (★corresponding to Claim 1)

As mentioned above, first invention is **a vertical parallel processor ("normal vertical parallel processor") comprising a coupled template, wherein plural input signals are given horizontally from directions on a surface situated in the middle of surrounding electrodes where the surface contains multilevel systems or neurons and output signals are taken vertically at different points on that surface.**

[0018] (★corresponding to Claim 2)

Here, plane shape of the above **template** on which multilevel systems can preferably be square or rectangular (see Fig.1-3). In such shape, plural input signals can be given horizontally p×q from all directions on a square or rectangular surface situated in the middle of surrounding p+q+p+q electrodes where the surface contains multilevel systems or neurons, and m×n dimensional output signal can be taken vertically at different points on that surface. Here the value of *m, n, p, q* are numbers varying from 0 to infinity, but both *m* and *n*, or both *p* and *q* cannot be zero simultaneously.

[0019] (★corresponding to Claim 3)

The plane shape of the above **template** on which multilevel systems can also be triangular, circular or polygonal (see Fig.16). In such shape, plural input signals can be given horizontally from all directions on a triangular, circular or polygonal surface situated in the middle of surrounding electrodes where the surface contains multilevel systems or neurons, and output signals can be taken vertically at different points on that surface.

When the plane shape of the above template is triangular, a+b+c(from three sides) input electrodes is set on the surface surrounding the triangle. When the plane shape of the above template is circular, n (number of input a along the perimeter) input electrodes is set on the surface surrounding the circle. When the plane shape of the above template is polygon of n sides, a+b+c+ …+n input(from n sides) electrodes is set on the surface surrounding the polygon. And, the processing surface and surrounding electrode height difference is varied for each processing surface.

[0020] (★corresponding to Claim 4)

In the above vertical parallel processor**,** the **template surface** is preferably conducting. And preferable **vertical electrodes** are those that measure STM (Scanning Tunneling Microscope) based tunneling current through multilevel systems or neurons

(see Fig.6). Here, the conducting surface is preferably ground and each electrode of p×q array is live and part of independent measuring circuit.

[0021] (★corresponding to Claim 5)

Another preferable **vertical electrodes** are ones that measure AFM (Atomic Force Microscope) based atomic force to come into contact with the multilevel systems or neurons. Here, the conducting surface is preferably ground and each vertical conducting tip of p×q electrode array is live and part of independent measuring circuit.

[0022] (★corresponding to Claim 6)

The **processing surface** of vertical parallel processor of this invention preferably has **thin films** comprising materials having redox active center or conformational sensitive center, containing at least two of the following properties A, B and C.

A. Materials incorporated between pair of electrodes show stable multilevel conductivity (Fig. 5C) at any particular bias in a definite range or application (see Fig. 5B).

B. Each state could be induced by applying different bias conditions (see Fig. 5B).

C. Transient current response to rectangular voltage pulse is an evoluted form of gaussian, or step or ramp or staircase one.

Here, “processing surface” means the surface of the template on which multilevel systems sit. And “at least two of the following properties A, B and C” means the case of (A and B), (B and C), (C and A), or (A and B and C).

As the above “materials having redox active center or conformational sensitive center, containing at least two of the above properties A, B and C”, we can give for examples, any molecular system, or systems comprising of nanowires, or nanoparticles, or quantum dots, or their organic or inorganic hybrids, or liquid crystalline materials or polymers, enzymes, lipids, DNA like different biomolecular systems and their hybrids, or any combination of organic materials and or with any inorganic composites, or pristine inorganic materials.

[0023] (★corresponding to Claim 7)

In the vertical parallel processor of this invention**,** said **multilevel system or neurons** comprises preferably the following means of A, B, C or D.

A. Sensor for specific signal detection and real world signals like sound, heat, light and any other form of energy when falls on the surface specifically designed sensor converts the signal into a 1D array of electronic signals;

B. Small processing unit of any other functional materials of specific function resulting in conversion of whole processing surface into different regions with different functionality;

C. Multilevel systems or neurons that can reversibly switch between all possible conducting states and remember the state more than the time of reaching equilibrium for whole surface (RAM) and refreshed as many times;

D. multilevel systems or neurons which once switch to one of the possible multilevel states remains permanently in the same state (ROM).

[0024] (★corresponding to Claim 8)

In the vertical parallel processor of this invention, **vertical electrodes** are preferably nanoscale width and macroscale length structure of similar heights with atomic edged tip where number of tips in one electrode system comprises preferably A or B.

A. One atomic edge to consider one solution point is single atomic edge tip (see Fig. 16),

B. Defined number of atomic edges in single electrode unit wherein solution point is average response of collective output for all individual atomic edges (seeFig. 16). Here, as the above vertical electrodes, we can give for examples, metal nanowires, semiconducting nanowires, carbon nanotubes, and any other metallic or semiconducting nanorod, nanotube or bundles.

[0025] (★corresponding to Claim 9)

In the vertical parallel processor of this invention, **inputs** are preferably connected to neural node controller (see Fig. 6) where all **input signals** are divided parallely into different unit preceding the processor and switching between each unit (see Fig. 7) containing A, B, C, D or E.

A. Unit that could vary the sequence order and intermediate ground connections;

B. Unit that permute the same arrayed input is into differently ordered array

C. Unit that passes arrayed input parallely through processor of different geometry to generate coupled output.

D. Unit that replace some of the input by pulsed array source

E. Unit that passes input signals through channels where signals are multiplied or divided to match with input impedance of whole processing surface

Here, the above neural node controller is hardware and software package which can modify the same arrayed input in different ways before sending it to the vertical processor.

[0026] (★corresponding to Claim 10)

In the vertical parallel processor of this invention, number of ground connection for p×q inputs varies (in region A of Fig. 6) preferably 1 to pq-1 to process same set of arrayed input; each combination of grounds preferably generates a specific node of operation and each node have preferably their own neural network so that after training and developing rules these nodes are used in different situations where a special kind of processing is required.

[0026] (★corresponding to Claim 11)

We can also use the invented vertical parallel processor reversely (reversed processor). When the neural model is reversed i.e. voltage is applied vertically and output is taken horizontally.

Namely, this invention also provides **a vertical parallel processor comprising a coupled template, wherein plural input is given vertically from top on a horizontal surface situated in the middle of surrounding electrodes where the surface containing multilevel systems or neurons and output signals are taken horizontally through the electrodes.**

[0027] (★corresponding to Claim 12)

In the above (reversibly used) vertical parallel processor, vertical plural input electrodes preferably have flat or spherical front edge generating local bias over large area on the processing surface, and front edge area of vertical electrodes preferably composes the following A, B, and C

A. Total area, which is sum of all individual vertical electrodes, cover more than a definite percentage of processing surface; wherefrom we generate nodes of input operations for every class of operations.

B. Relative area of electrode bundle or individual vertical electrode varied tuning control of individual input on final solution surface.

C. Front edge geometry modified to tune potential distribution of the contours on processing surface.

[0028] (★corresponding to Claim 13)

As mentioned above, second invention is **a cluster (see Fig. 18) which comprises the above normal vertical parallel processors;**
neural node controller; and
connections motors sensors connected following ways A, B and C.

A. Some or all of the processors input connected to an array of vertical processors, rest of them to output of sensors which are free input of the whole system;

B. Some of its output connected to some of the output motors and rest of them connected to other vertical processors;

C. All free outputs connected to motors and not connected to any input of the whole system, taken vertically as a final cluster output.

[0029] (★corresponding to Claim 14)

As mentioned above, third invention is **a modified virtual source neural network model (see Fig. 11) which comprises any one of the above vertical parallel processor, and its modification contains all of the following A, B and C.**

A. Binary neuron (having value 0 or 1) or continuum neurons (any value 0 to 1) of old concepts is replaced by multilevel system or neurons (selected values between 0 to 1).

B. Introduction of virtual sources as effective input to each neuron does not come from other neurons.

C. Modification is accession to individual outputs as we take output vertically; hence model becomes a 3D (3 dimensional) model.

This invented virtual source neural network model has been developed from Hopfield principle of 1982 (see Fig. 11) to fit with the above vertical parallel processor. Here, "model" means a set of basic principle, trick or rules to be followed during development of training software for real time operations.

[0030] (★corresponding to Claim 15)

In the above model, its configuration can be developed (see Fig. 14) by minimization of an energy term containing vector sum of the products of weight generated by effective inputs from virtual sources or global weightage and vertical probe generated weight or local weightage and these two positive contributions can be negated with weightage generated by the threshold value of multilevel states.

[0031] (★corresponding to Claim 16)

One preferred embodiment of the above model contains A, B, and/or C.

A. feed-forward network by connecting some or all output of the vertical parallel processor model back to its own input directly or indirectly (see Fig. 12);

B. model with one or more hidden layers (see Fig. 11) of multilevel neurons and generating lower or equal number of output at different levels to reach final output;

C. intermediate layers (see Fig. 11) composed of mixed multilevel logic neurons, which comprise more than one kind of logical neurons together like tetranary or octanary systems or other logical systems.

[0032]

As mentioned above, forth invention is **a processor training method (see Fig. 12) to train single vertical parallel processor of the above invented vertical parallel processor, where input and output are correlated by the above invented artificial neural network model finding rule or weight coefficients of virtual neurons or multilevel systems following major initialization of the below training steps (1)-(3).**

(1) Firstly finding range of application (see Fig. 13) for local bias and global bias;

(2) secondly finding their levels of operations or functional behavior for each multilevel logic states (see Fig. 13);

(3) finally developing (or finding) logical function by energy minimization so that when an unpredictable input is given it can give most probable solution of the problem (see Fig. 14).

[0033] (★corresponding to Claim 18)

In the above processor training method processor, developing logical function in above step (3) for performing mathematical operations (see Fig. 17), preferably comprises A or B addressing functional criteria containing C or D.

A. Via concept of matrix inversion process, where 3D matrix inversion to linearized array for vertical input horizontal output of the invented **(normal) vertical parallel processor.**

B. Via linearized array to 3D matrix conversion for horizontal input and vertical output; which is basic operation method for the processor of reversed **vertical parallel** processor.

C. Probe bias is used as operator to treat mathematical functions.

D. Number of ground connection for p×q inputs varies 1 to pq-1 to process same set of arrayed input; each combination of grounds generates a specific node of operation and each node have their own neural network so that after training and developing rules these nodes are used in different situations where a special kind of processing is required.) with geometrical processing surface variation of the above invented normal or reversed vertical parallel processor is used to generate specific functional criteria.

Here, as the above mathematical operations, we give, for example, mathematical operations like matrix conversions, operators, tensor treatment, integration and other functionalities.

[0034] (★corresponding to Claim 19)

In the above processor training method processor for the above clusters (see Fig. 18-19), training is preferably done following the above model containing basic considerations A, B, and C.

A. Input of the processor is free input of the cluster considered as 2D input array, output of the processor is final output of the cluster considered as 3D array and all basic processor components of cluster is replaced by one or more layer of multilevel neurons.

B. Individual components of the cluster are trained first and then its importance in final output is determined by finding functional relationship with most similar part in final output pattern.

C. As there are two different kinds of inputs in clusters, directly from sensors or from any other processors hence importance of two different kinds of inputs to the final pattern is determined by finding functional relationship.

[0035] (★corresponding to Claim 20)

In the above processor training method for the above reverse processors, training is preferably done comprising steps A, B and C

A. finding range of application for local bias and global bias with additional criteria of crosschecking reproducibility of neurons in the contour on processing surface generated by field projection from vertical electrodes.

B. finding functional behavior for transition to each multilevel state along with field distribution contour generated by interplaying of neighboring vertical electrodes.

C. developing logical functions by energy minimization considering minimum energy path from one horizontal electrode to another.

[0036]

In our dynamic brain there are continuous changes of connectivity, enables it to develop some basic rules, which are implemented in unknown situations. Developing rules are nothing but making permanent changes in a 3D processor network. But whatever solid-state devices we create we cannot change the configuration of the system and hence the equivalent solid-state system should have three basic criteria. First, it will be a system with extreme parallel processing; i.e. death of any element on its processing path or noise should not have significant impact on the final decision-making. Secondly, it should be able to generate a 3D pattern solution to provide collective output of the superimposed signals. Finally the working principle of built in processor should be flexible to be modified or converted into a processor of different functionality, configured as RAM and ROM based processors, sensors of unique operations etc. Not only that working principle should support all kinds of versatile data should be processed in a single processing unit i.e. all kinds of signals coming from functionally different sources superimpose during acquisition of the data but still it should not dilute those data as a part of its own data processing.

[Preferred Embodiment of Invention]

[0037]

Fig.1 shows schematic presentation for the vertical processor of this invention. Horizontal and vertical parts are electronically and physically independent and shown in coupled position. And, Fig.2 shows horizontal surface design stages and its external connection and Fig.3 shows vertical surface design stages with its external connections shown in Fig.1 respectively.

The working principle of our model processor of the present invention could satisfy all the basic requirements as described above. Before describing the invention model and method we describe the model device that can implement this principle for clarity. The processor has two templates one processing surface unit **101** and other vertical electrode array unit **102** facing each other. Cables from each vertical electrodes **103** and horizontal electrodes **104** bundles out for input or output from processing surface **105** or acquisition surface **106**. Processing surface has neurons **107** and vertical electrodes are at a tunneling distance from the neurons. There is always a gap between processing surface and the electrodes **108** confirming no tunneling and its ground is also connected to the output **109**. We need to create electric field distribution on a horizontal surface; hence outer electrode thickness d_1 **201** should be higher than the thickness of the horizontal conducting surface d_2 **202**. The combination metal electrode surface and substrate depends on the kind of neuron is being used and also the technology used for

fabricating the structure. As an example we take Si(111) substrate of low resistance **203** depositing SiO_2 by chemical vapor deposition **204** and finally depositing outer Au electrodes *E* by e-beam lithography **205**. Then we lift off SiO_2 by dry etching **206 207** and finally we deposit the Au processing surface *P* **208**. The present structure is part of a larger structure where each electrode along with the processing surface or ground is connected to the outer circuit **209**. The dimension of the electrode array $p \times q$ or $m \times n$ is determined by system requirement **210**. The Au surface is made atomically flat by H_2 annealing. So two stage lithography is required for realizing this. Vertical electrode array is not a necessity for the present invention but could be useful for commercial application. For the vertical electrode array we take low resistance Si(111) plane **301** deposit SiO_2 by chemical vapor deposition **302** a pattern of Au as in Fig.3B is deposited on top of this by e-beam lithography **303** and the entire surface is covered with resin **304** and some part is dry etched **305** so that we can grow isolated nanorod or nanowire array in the selected region only **306**. The whole process as described in Fig.3A could be done on a high resistance Si substrate without depositing SiO_2. We may need to spin cast catalyst metal between **305** and **306** for initiating nanowire or nanorod growth. Vertical growths of nanowire for different metals and semi conducting materials have standard methods established in published works via growing chemical bath deposition, chemical vapor deposition etc. All electrode connections are part of a large structure whereby they are taken outside to external electronic circuit.

[0038]

The sample is replaced by horizontal processing unit **401** in any STM/AFM set up (Fig.4) wherefrom one can taken $m \times n$ cables out of the system **402** and connect it to the voltage sources with PC based GPIB/RS control system. Dedicated software may control pulse or magnitude or time of application input. Vertical output is generally STM or AFM tip **403** connected to original STM/AFM body **404** as far as applicability of the present invention model is concerned. We may design dedicated two piezo motor based system back to back for the present coupling system **405**. For commercial application the vertical electrode bundle similar to the design we have proposed could replace tip **406 407** in the main STM/AFM body **408**. Vertical electrode bundle case could be considered as a very typical case of our invention as its theoretical modeling is very much limited. For the vertical output we take $p \times q$ cables out of the system **406** and each output have independent current measuring unit with horizontal surface as their common ground. During approach **409, 410, 411** one or more of the output is connected to tip positive and ground is the tip ground. As soon as the tunneling current is received it is considered that some of the electrodes have come near to the tunneling distance. By moving the substrate or tunneling electrode position we make the vertical and horizontal part into right position. We suggest a simple trick to get into right position in Fig.4C. Any one of the four switches *S*1, *S*2, *S*3, *S*4 is switched on and scanning is performed inside the STM system based on point A', B', C', D'. We try to increase the common region **412, 413, 414** till we reach the deserved processing surface i.e. maximum common region. As it is not possible in the present technology to prepare all electrodes vertically in the same height we cannot guarantee how many of them is connected or which system is acquiring highest output. Also mostly electrode responses are also non-linear. But this system is capable of showing that bits are processed simultaneously and helps in developing concept for commercial unit where a fixer used **415** to fix the horizontal and vertical unit

at the tunneling distance **416** after getting into maximum common region. Thus we built the concept device for horizontal input vertical output and vice-versa.

[0039]

As we have built the concept for a box, which could implement our present invention, we need concept building for the neuron, which can have multilevel conductance state. The word 'neuron' signifies the equivalent system composed of any material but behaving as a unit on the horizontal surface and showing multilevel conductivity. The word multilevel conductivity signifies that the equivalent unit system could be switched to states of different conductivity and at a particular probe bias measured conductivity would be different after switching. By acquiring or donating electron or by conformational change the system can stay in different energy (U_{ij}) minima of the configuration space (q_{ij})(Fig.5A). Each energy minima corresponds to a conductivity of a system **501**, **502**; and also a multilevel state **503, 504**. The conductivity difference of different state should be large. We need to prepare films using organic or inorganic materials that can produce systems of multilevel conductivity on the horizontal surface. Following this basic criteria we can select many systems. We might select molecules that show multiple electron reversible oxidation-reductions in cyclic voltametry so that every electron acceptance or donation could lead molecular systems into different conducting state. We might select nanowires anchored with oxidizing/reducing legands or molecules, so that varying the degree of oxidation or reduction multilevel systems could be realized. Molecular systems like DNA, polymers or long chain molecules, biomolecules having conjugation along its length anchored to switching molecules or nanoparticles or oxidizing/reducing agent are some of the examples where we can have multiple oxidation or reduction states or conformational states with different conductivity could be regarded as multistate systems. Such films are grown by self-assembly and conformation changes are controlled by different parameters till we reach the most desired system of our choice. Multistate systems have a definite energy required for every state, which are supplied by electric field. When a sequence of voltage is applied **505** inducing different conducting states **506** and probing several times in between **507** with similar probe bias we should find different conductivities for every sequence of probes **508**. The written state could be erased by applying suitable pulse **509** clear declinations in the state **510** would be obvious. If the system is irreversible then the system could be used as a ROM and we could use one neuron only once. Any system fabricated as above, shows the "write-read-erase-read" property as analysed is regarded as neuron of multilevel states.

[0040]

The operational network for the whole testing system have two coupling circuit horizontal and vertical(Fig.6). Horizontal processing surface **601** connected to neural node controller **603** via *mn* cables **602** and output of neural node controller could be connected to independent voltage sources **604** or sensor array. Different functional sensor array *F1, F2, F3, F4* **605** could be connected to neural node controller. The output is read by scanning response of all neurons **606** with STM tip Fig.6C, also we can measure the output by an array of independent current meters **607** Fig.6D or even connect them to the motors **608** Fig.6B. Now we need a discussion on the neural node controller (NNC) (Fig.7) that is an interface between sensor/source **701,702** and modified nodal input for the horizontal processing surface **703,704**. There are two aspects of NNC. In general

variation of electric field distribution by effective source $\{I_n\}$ on a particular point of the processing surface **705** follows some rules if the number and orientation of ground connection is fixed, geometry of processing surface is either circular or triangle or polygon, i.e. any defined geometry. Second, for a specific composition of organic and inorganic material i.e. virtual neuron the response function changes reflecting the mysterious features of supramolecule. The objective of neural node controller is to take signal source $\{S_n\}$ and vary ground connection, external bias, pulse sequence, pattern control and creating different routes by hardware so that when signal passes through it creates completely new defined routes of voltage variation. Only random variation of signal sources $\{S_n\}$ could create unique electric field distribution following a defined rule; hence neuron response function i.e. relation between original input and output of neuron would be more specifically defined. We create different electric circuit capable of generating $\{I_n\}$ set of signals to the horizontal processing surface from $\{S_n\}$ set of sources. Every set is seed for random electric field distribution on the surface and called neural nodes; we can switch between nodes *N1, N2, N3…Nn* **706**. Each node corresponds to a function *F1, F2,…, Fn*, **707** and all these functions could be generalized to make final reference function *F* **708**. We carried out electric field distribution on a rectangular surface including lines of forces **801** and isopotential surface **802**. Ground connections denoted by *G* in column C of Fig.8 and in some cases of column A and B of Fig.8 shows that ground connections determines the basic and most prominent features of electric field distribution. As soon as electric field distribution is created the processing surface neurons responds to the field and attempts to reach equilibrium conformation. The dimension of the quantum well **901,902** allowed determines the level of conducting neuron conformation (σ_n) would be allowed in each well. In other words dimension of the 3D box **903** determines which conducting balls to be fit in **904**. STM/AFM tip tunnels current for each box packed with neuron ball and creates different height **906, 907, 908**. All these Nanoscale columns of multilevel response give rise to a surface **909** at microscale. Every peak on this surface could be regarded as a solution to the input signal mystery. So from real world sensors like light sound heat signal is transformed to an array of electronic signal **1001** and all these arrays are fed into horizontal surface **1002**. This signal generates electric field distribution, multistate neurons interact and reach equilibrium **1003** random distribution of 3D quantum well with a neuron in it **1004** compels it to reach only allowed states. Array of vertical electrode **1005** applies small voltage to read the neural states without destroying the 3D well **1006**. Resultant 3D array of output can control motors connected **1007** in multilevel way **1008**. The realistic model of Neural Network develops logical relation **1009** between input array of electronic pulse **1002** and output 3D array **1006**. This relation is used to predict results in unknown situations.

[0041]

We develop our invention model as follows: We consider each multistate system on the processor as a neuron **1101,1102,1103** that can have conductivity at a particular composition of virtual source **1104,1105,1106** and it is switched to different states. At any instant of time the state of the neural network surface is 2 dimension m×n component matrix $V=[V_{11},V_{21},V_{31}…V_{mn}]$ where there are *mn* multistate system on the surface. The value of components ranges from *0* to *n-1*. So we change from Hopfield's probabilistic discrete model and deterministic continuous model in a sense that output acitivity of

neuron X_j is a time dependent multinary parameter equaling *0* to *n-1*: $X_j(t) = (())V(n-1)$ where *V(n-1)* is a logical or function of *n* input and one output **1107**. Unlike standard neural network model here we don't have presynaptic neuron instead we have a element of potential and field distribution matrix χ_{ij} i.e. the virtual source impact **1108** for each neuron input, which are generated by electric signal of surrounding electrode array. But we have synaptic connection weight W_{ij} for the neuron to give output, which depends on the effective potential between the ground and the tip, interaction between individual elements and with the tip. When we consider multilevel logic we have *n* threshold values for each state to realize. Considering each neuron threshold values are randomly distributed in the range of voltage applied and we can consider a set of threshold voltages $\{\theta_i\}$ for a given system. Output of a neuron **1109** is a function depending on the field matrix element as input, multistate threshold values, transition probability in the matrix, response function measured individually. Our invention modifies 20 years old neural network concept by (a) removing presynaptic neuron introducing virtual source, (b) introducing multilevel logic (c) considering individual output.

[0042]

Now we can write each element of output tunneling current pulse measured by vertical electrode or bundle of nanowire is basically a gaussian function $f(x)$, e.g. for NDR (negative differential resistance) system given by:

$f(x) = \frac{1}{\sqrt{2\pi\sigma}} \exp\left(-\frac{1}{2}\left(\frac{\upsilon - x}{\sigma} \right)^2 \right)$, The output function could be a step function or ramp function or sigmoid function etc. depending on the kind of input voltage pulses applied to the system. The variable x of this function depends on weighted average of the synaptic input from surrounding electrode array, probe bias from nanowire tunneling current measuring circuit and threshold for multistate switching.

$I_{ij} = f\left(\sum_{k=1}^{e} W_{ijk} \frac{V_{ijk}}{r_k} + V_p - \theta_k \right)$ Where *ij* is the co-ordinate of the neuron on the processing surface where current is measured and *k* is the rank of input electrode of total *e* electrodes, each at a minimum distance of r_k. V_p is the probe voltage and θ_k is the threshold for k^{th} state. Here we neglect excess electronic state modification due to clustering of multistate systems and defects of geometrical surface, but intersystem interaction is considered in synaptic weight.

Every multistate system or neuron on the processing surface have most probable state θ_k for which energy of the state becomes minimum for a given weight. The energy of the system is given by

$E = -1/2 \sum_{ijk} s_k s_{ij} w_{ij} - \sum_{kp} s_k V_p + \sum_{km} s_k \theta_m$ The energy variation is controlled by probe bias and threshold as it is a multilevel neuron, here s_k is effective potential for the electrodes i.e. virtual neurons. Based on this expression of energy logic dominating state is determined and we find weight variation with θ_m. Sets of most probable states are used to determine how neurons are capable of generating multilevel logic in the system. For an example if we have 8 level logic, θ_m varies 0 to 7. And 3+5=0, 5+5=2 in this system. So

after application of an array of voltages from outer electrodes we get a random distribution of number varying 0 to 7 on the processing surface.

[0043]

After selection of θ_k output error for each is calculated and most probable weight are chosen by backpropagation algorithm i.e. calculation continued by feedback of resultant weight till error is minimum. We can consider hidden neuron levels between the processing surface and output layer **1110,** here we discuss only one hidden layer. If we have input node **1111, 1113** as *pq*, hidden node **1110, 1114** as *st* and finally output node **1115** as *ij*. In the hidden mode it could be our model neuron **1114** or Hopfield neuron **1110**. The whole processing surface is divided into *mn* cells as there are *mn* number of input electrodes. But each of the *mn* cells can have several multistate systems, say the number is *ab*. V_{pq} is input for each of the input cells and *pq* varies from 11 (p=1, q=1) to *ab*. The output of these cells are given by $V_{st} = f\left(\sum_{p=1,q=1}^{ab} W_{stpq} V_{pq} \right)$, so if there are *cd* hidden layer of neurons then *st* varies *11* (*s=1,t=1*) to *cd*. Now we have only one output I_{ij} for STM/AFM or only a few say *uv* number of output copying bundle of nanowire or nanorod or nanotube electrode which might replace STM/AFM tip. Hence $V_{ij} = f\left(\sum_{s=1,t=1}^{cd} W_{ijst} V_{st} \right)$ so finally the output for the modeled neural system becomes:

$$V_{ij} = f\left(\sum_{s=1,t=1}^{cd} W_{ijst} f\left(\sum_{p=1,q=1}^{ab} W_{stpq} V_{pq} \right) \right)$$

[0044]

We can introduce the concept of threshold voltage θ_k and probe voltage V_p to this function as earlier. Now we discuss implementation of the above principles in programming. First we need to find θ_k and also weight combination corresponding to each state; how such a state is derived in a cyclic way? In other words we would like to use the system as analogue to digital converter where for any random voltage array input, we always get output varying 0 to 7 for 8 level logic system. The cyclic operations may not be straightforward, as we may need to develop a few rules describing how we change logical response for a particlar region simply by changing some input bias. This will establish coherence with normal day computer processor.

[0045]

First we have to determine potential sum range $V_{iL} < \sum V_i / r_i < V_{iH}$, in which output response is sensitive for a particular probe bias V_p, where V_{iL} is lowest potential sum below which no neuron can respond on the surface **1201**, V_{iH} is highest potential beyond which noise overshadows significant changes **1202**. Similarly we have to determine range of probe potential V_p lowest wherein determines the minimum voltage required to probe a neuron **1203** and highest voltage is the magnitude beyond which electrode potential changes become insignificant **1204**. Secondly a neuron cannot be very sensitive on all logical states then its ranges of logical states and finally potential sum required for achieving each state for each neuron. In our case as we have multistate system we need to check energy minimum or potential sum for the threshold and the synaptic weight. We have determined how potential sum or weight varies for a particular

state with change in nodes for a particular neuron in Fig.13A,B. The average of nodal effect is plotted in Fig.13C to determine most probable array combination to be selected for inducing a particular state to a particular neuron. From this array arrays of heighest probability of inducing are selected in Fig.13D and applied in all possible combination to develop the rule of multilevel logic in Fig.13E.

[0046]

We have summarized the step-by-step procedure for the training process, which could be realized in many possible ways. In our case here we have described a very special case by considering that there are no hidden neurons in the neural network in Fig 14. Our energy variable is three sets of parameters and target is to find the activation and most probable state for any given input sequences of signal. So we minimize energy **1401** or from earlier steps **1402** we determine function for multilevel state variation **1403** G_{ij}. We replace inverse function determining threshold in the main expression for the output **1404** that our model device whenever encounters any unknown set of input signal can respond according to the necessity if motors are connected according to the learning of its inherent nature. As in our model probe, horizontal electrode and threshold voltage all are varying hence whole minimization of error could be repeated a few times by back propagation algorithm considering first set of parameters for synaptic weight and probe effect as initialized values for second minimization process.

[0047]

Vertical accession of output data simultaneously with molecular scale resolution is not possible, as we cannot take out so many cables from such a small area. We access output by STM in reality to prove our invention model experimentally. As STM have only one tip, so we compromise with simultaneity and rely on memory of multistate systems as complete set of output is generated only after finishing the scan.

To prove the model we have applied steady state voltage array in the input electrodes instead of pulse; hence STM/AFM tip current is basically a ramp or sigmoid function, considering a sigmoid function $f(x)$ given by $f(x)=\frac{1}{1+\exp(-ax)}$ where a is the slope parameter of sigmoid function. As soon as we study our multistate neuron and vertical network concept with STM we can study theoretical concept of hidden neuron experimentally. Because STM can scan all over the surface hence every multistate system on the surface is probed as everyone of them receives specific potential and electric field from the external surrounded electrode array. As a result number of output is much smaller than the input. Higher is the data accession resolution more efficient is the device and hence less is the difference between number of multistate system and number of output.

[0048]

Error generated after selection of each weight is feedback to the input and input value is corrected, the error is basically MSE i.e. Mean Square Error. If more hidden layers created based on the above mathematical trick then error function changes accordingly. On the processing surface, during operation errors generated are normally transported horizontally hence vertical contribution is minimum. Again, as the system is not sequential hence spatial distribution of error function needs to over shadow neural response over all regions to mask resultant pattern. In Fig.15A we have plotted the resultant lines of forces for the input signal and connected most significant solution

points $S_1, S_2, S_3 \ldots S_n$ on the surface. Now even if each individual vectors are modified they cannot change the connecting pattern solution the reason is no error can work in harmony all over the surface. For this simple logic our processor can survive under extreme noise like our brain. Also by introducing the concept of hidden neurons **1502,** we can neutralize the error mediated decision changes. Also downsizing the neural decision making cluster can reduce noise mediated decision changes **1503**.

[0049]

Finally we would like to discuss some of the real time parameters and their importance in our model device, which we bypass completely by ANN while analyzing solutions. When a set of electric bias is applied to the processing surface we have a potential at every point on the surface. In general we consider that there is no multistate systems on the processing surface or the processing surface is a surface of constant conductivity then the potential $\phi(x, y)$ in the entire region outside the electrodes is the solution of Laplace's equation. $\nabla^2\phi(x, y) = 0$

For the simplicity we consider a circular processing surface of radius b and surrounded by 16 electrode of radius a, by superposition principle the total potential at any point on the surface is sum generated by each electrode.

$$\varphi(z) = \sum_{n=1}^{16} \phi_n(z), \text{ Where } z=x+iy \text{ and } \phi_n(z) = C_n \log\frac{a}{z - z_n} + \sum_{k=1}^{\infty} A_{nk}\left(\frac{a}{z - z_n}\right)^k$$

[0050]

In this expansion, the first term represents a potential established by a monopol located inside the n^{th} electrode, *k* corresponds to the dipole, quadrupole, octapole moments of uneven charge distribution on the n^{th} electrode. By boundary conditions we can determine the value of *C* in terms of *a* and *b*.

Now we place multistate systems on the processing surface. We find that during application of various electric signals there are charge distributions on the surface. But as we measure output current by STM we take into account quantum dynamic effect of the uneven charges on the potential surface but may not change the Laplace's equation. Using quantum path-integral molecular dynamics (*QUPID*) which rests on discrete version of Feynman's path integral method an electron interacting with *N* particle cluster

$V_{eff} = \sum_{i=1}^{P}\left[\frac{Pm}{2\hbar^2\beta^2}(\vec{r}_1 - \vec{r}_{i+1})^2 + \frac{1}{P}V_e(\vec{r}_i)\right]$, where *P* is the number of contributions taken into account as a superposition of a harmonic potential and the cluster potential. When we measure the tunneling current, effective sample bias becomes sum of potential generated by surface electrode and effective potential generated by classical ions:

$\phi_{sample} = \phi_z + < V_{eff} >$, Height of the barrier is approximately average of the sample and the tip bias. $\phi_{barrier} = 1/2(\phi_{sample} + \phi_{tip})$, so current can be expressed by

$I \propto V\rho_{sa}(0, E_F)e^{-2kd}$, with $k = \frac{\sqrt{2m(\phi_{barrier} - E)}}{\hbar}$, *E* being energy, ρ being local density of states. Here tip bias generated field is local player and surrounded electrode generated electric field is global player, they interplay with each other and we choose the values of both in such a way that external modification of conductivity by electric field is more significant in the proposed model of realization. Normally the order of electric field

in the tip is ~$10^8 V/m$ (e.g. $1V/2nm$) and electric field modifies conductivity of the order ~$10^6 V/m$ only by thermal hopping and conductivity increases with field $\sigma = \sigma_0 \left(\frac{e^3 E}{4\pi\varepsilon_0 \varepsilon k_B^2 T^2} \right)^{1/2}$. Hence external electric field should be more than that i.e. of the order of ~10^7 V/m so as to significantly contribute to the tip bias but not completely overshadow it. Then tunneling current is nothing but noise. Hence for an example if we have 16-electrode system separated by $1000nm$ distance then if at a point on the processing surface every electrode contributes $+5V$ then we have ~$8\times10^7 V/m$. So the device operational voltage range needs to be optimized based on the film thickness, electronic character of multistate systems used, tip bias, molecular surface conformation and processing surface geometry.

[0051]

In Bardeen's approach $I = \frac{2\pi e}{\hbar} \sum_{\mu,\nu} \left[f(E_\mu) - f(E_\nu) \right] \left| M_{\mu,\nu} \right|^2 \delta(E_V + V - E_\mu)$ Where $f(E)$ is the fermi function, V is again the applied voltage, $M_{\mu\nu}$ is the tunneling matrix element between the states and depends on wave vector k which in turn depends on $\phi_{barrier}$ and E is energy of corresponding states.

In non-equilibrium green function formalism (*NEGF*) there is a virtual reservoir **1504** connected to conductor **1505** which is conceptually hanging between atomic surface **1506** and STM/AFM tip or vertical electrode **1507**. the potential term for the Hamiltonian operator H_C is given by $U(r) = \phi_{sample} + \phi_{tip}$. Hamiltonian operator H_C is used to determine the Green's function $G^R = \left[EI - H_C - \sum^R \right]^{-1}$, $G^A = \left[G^R \right]^+$. The current is given by

$$I = \frac{2e}{h} \int_{-\infty}^{+\infty} \left[Tr\left(\Gamma_1 G \Gamma_2 G^+ \right) \left(f(E,\mu_1) - f(E,\mu_2) \right) \right] dE$$

[0052]

In spite of taking into account various parameters, direct prediction of output and its transition to different states is not possible. Several parameters like defects of the atomic flat surface, existence of different planes, variable intermolecular interactions, fluctuation in transition probability of multistate systems at different states cannot be incorporated in these computation process for fruitful realistic prediction. Hence we can avoid all these parameters in ANN based concepts as we discussed above. Also we can change processing surface as triangle **1601**, rectangle **1602**, polygon of *n* sides **1603**, circular **1604**, then the logical response change of the surface becomes more and more complex and almost impossible task be taken into account without ANN.

Now we would like to make some comment on versatility of the processor. First is reversible use. When the neural model is reversed i.e. voltage is applied vertically and output is taken horizontally then following the proposed neural network model we get results but we do need to change training process as STM/AFM tip creates random local path tuning. The real physical explanation of the system as discussed above is not valid in this case as horizontal processing of signal is a dominant physical phenomena which is insignificant in the above theory we presented. So ANN provides positive result but versatility is not possible to incorporate in the present model. Secondly we scan all over

the surface **1606** with STM/AFM tip **1605** to find result. So we get maximum number of solution point in this case. When we use vertical electrode array then considering engineering constraint, for one tip **1608** we have surface of single dots **1609**, for four tips **1610** we have a surface with localized cluster effect of four points **1611**, for eight tips **1612** we have a surface with localized cluster effect of eight points **1613**. If we plot the efficiency *E* of the device with variation of probe number *n* then initially efficiency increases as average response is taken into account but if *n* increases to a higher value then interaction between probes decreases efficiency of the device **1614**.

The present invention model is itself a complete example of matrix linearization Fig.17A. Even reverse operation is achievable by changing input/output configuration. Once we have determined how to modify localized solution pattern Fig.13E we can develop rules for individual mathematical functions Fig.17B. So we generate a set of weight factors that predicts mathematical operations. The processor is compatible to carry out quantum mechanical computation, e.g. operator functions. We train probe bias as operator to develop rules for quantum mechanical algebraic operations Fig.17C.

[0053]

As we develop the concept of vertical processor, combination of several processors for the grand output matrix of the whole system is an immediate application in Fig.18 could be developed. Any kind of processor input can get connected with any other kind of processor but any output to get connected to any input significantly we need to have manual converter to supply equivalent voltage to the respective input **1801**. ROM processors are **1901** connected randomly with RAM processors **1902** and vertical projection of the connectivity also gives a matrix whose some of the elements are fixed due to ROM. The 3D matrix of processors inside the wall ABCD-EFGH in Fig.19 have projection of output connection on the ABCD surface; hence the output coming out of the surface vertically is basically “vertical output” as we discussed above. We can apply the same concept by correlating matrix seeds **1903** of output matrix cluster **1904** in the larger random integration of processors of different dimension or functionality. Hence the final processor follows the principle of vertical accession from random 3D input sources as the above-discussed theory. There are only two basic changes; first is that weightage function for synaptic input by virtual sources are now weightage factor of processor output matrix on its input and results in output matrix elements which becomes seeds of another matrix. We can also apply projection theorem to find the effective output from a random cluster. Hence the concept of horizontal input vertical output and vertical input horizontal output is a universal concept in developing a fuzzy neural network system into brain like processor of future.

[Short Figure Captions]

[0054]

[Fig.1]

Schematic presentation for the vertical processor of this invention. Horizontal and vertical parts are electronically and physically independent and shown in coupled position.

[Fig.2]

Horizontal surface design stages and its external connection of the vertical processor shown in Fig.1.

A shows schematic presentation of major steps to fabricate template of horizontal surface. B shows the final structure to be built of p×q dimension. C shows external leads created by photolithography or direct metal mask deposition for external electronic circuit interface with horizontal surface.

[Fig.3]

Vertical surface design stages with its external connections of the vertical processor as shown in Fig.1.

A shows schematic presentation of major steps to fabricate template of vertical surface to replace STM/AFM tip and for commercial applications. B shows final vertical electrode array template. C shows external leads created by photolithography or direct metal mask deposition.

[Fig.4]

Connection and setting up of the characterization unit to check the proposed model of this invention. A. Schematic of a STM/AFM unit where sample is replaced by *mn* cable network connected to horizontal processing surface. B. Schematic of standalone system of this invention. C. Schematic of accurate coupling between horizontal and vertical processor of this invention.

[Fig.5]

Selection of a smart system to be used in the processor. A. Schematic energy diagram for smart systems or neurons of this invention.

B. Schematic of testing of smart systems; performing multilevel RAM or "write-read-erase-read" multilevel process of this invention.

[0055]

[Fig.6]

Schematic of the proposed hardware control unit for real world application of this invention. A. Electronic circuit for creating unique electric field distribution via neural node controller. B. Vertical electrodes each connection to motors could be controlled by PC4. C. Circuit of reading solution via STM/AFM, or model testing circuit. D. Vertical electrode readings could be seen directly through independent current meter. E. Unique horizontal electric field distribution creation via functional sensors; this could be connected before or after neural node controller.

[Fig.7]

Neural node controller of this invention. A. Different ways of generating neural nodes. B. Usage of neural node controller by different modes.

[Fig.8]

Theoretical simulation results of electric field distribution on horizontal processing surface with 16 electrodes a particular case of this invention. A. Simulation for different ground connections for set of higher voltage range. B. Simulation for different ground connection for set of lower voltage ranges.

[Fig.9]

Schematic of operation mechanism of a model processor of this invention.

[Fig.10]

Diagram for real world operation of the processor of and simultaneous ANN training of this invention.

[0056]

[Fig.11]

The concept of models. Top three electrodes shows schematic of virtual source concept which leads to our model of this invention as directed by arrows. Our model is essentially different from Hopfield 1982 neural model of prior arts as described in reference [non-patent ref. 1]. Below is schematic of neuron equivalency including hidden layer of this invention.

[Fig.12]

Finding range and domain of application for a real processor of this invention.

[Fig.13]

Determination of rule for tuning specific states of neurons in a much localized region of a real processor of this invention. A. Schematic for the determination of performance level classification of the processor. B. Multilevel generated classification of neuron response, a schematic behavior. C. Classification of potential response, schematic behavior for a particular input set. D. Determination of minimum response array for a particular state. E. Determination of the rules.

[Fig.14]

Training process of the processor of this invention.

[Fig.15]

Survival of processor output under noise and real parameters that tune output of the processor. A. Dealing with noise of the processor in this invention. B. Schematic of real parameters controlling performance of the processor of this invention. C. Schematic of NEGF formulations of non-patent ref. 7.

[0057]

[Fig.16]

Versatility of processing surface and tip effects of the processor in this invention. Schematic presentation also shows coverage of solution surface for different cases while STM/AFM case being the best.

[Fig.17]

Mathematical operations using vertical processor of this invention.

[Fig.18]

Constraints and connectivity versatility of the vertical processor of this invention with many similar kind of processors of this invention.

[Fig.19]

Universatility of the vertical accession concept of this invention in building concept of giant processor network using processors of this invention.

[Example]

1. We have made most basic of the processor described above; horizontal basic p×q as 1×0 which means global control is done by external two electrode one opposite to another while processing surface is in between and data taken vertically by STM. And we have successfully tested whether dual mode tuning is done or not. Then we increased 1 electrode to make $p \times q$ as 1×1, we call third electrode as r. The system was made as follows. We begin with template as mentioned above fabricated by the combination of e–beam lithography and e-beam evaporation of gold on Si(111) substrate where horizontal electrode couple (height of p, q and r~100 nm) and processing surface in between (height for processing surface~50 nm) is isolated by ~80nm. Increasing electric bias within certain limit could not induce charge injection to the processing surface as the gap was

theoretically simulated keeping it beyond critical limit. Nanoscale two-stage lithography to generate a height difference of ~50nm between electrode and processing surface decreased success rate of final pattern around 30%. Processing surface area varied between 100-200 nm^2. Large area atomic flat surface of (r.m.s. <1.5nm) and symmetric STM tip (electrochemical etching followed by structure investigation) was essential for global tuning of quantum phenomena. After fabricating gold template on Si(111) wafer as above we anneal the substrate in a quartz chamber 100% H_2 flow at rate 60mL/min. This is followed by annealing at temperature 400^o C (600^o C for gold on freshly cleaved mica) with rise at rate 15 degree/min, stabilize for 30min and sudden switching off the heat source to cool down. The substrate kept at an optimized angle of 15^o in the best operational range of 9^o to 22^o with horizontal axis facing the H_2 gas flow. Which is very crucial to generate large area reconstructed atomic flat gold Au(111) substrate. To minimize defect further the template is dipped in DMF solution with continuous tilting of solution with horizontal axis at rate 3 degree/sec for 60min and no tilting for 2hrs. The cycle repeated 3 times followed by H_2 annealing as described above. The method describe can generate large area atomic flat surface (~500nm^2 with r.m.s ~8 nm) with less defects than any one methods. Survival of final template was around 10%.

Freshly annealed template was soaked in micromolar ethanolic solution of *RB* (Rose Bengal) for 5 hours to give rise to 1.2 monolayer coverage self-assembled film of r.m.s. ~1.5nm thickness. Quantum hole at specific locations were observed at different sections on the surface coverage. Optimized design and fabrication of a dedicated electrode system helped to locally perturbing the system (vertically) by STM, while stabilizing its environment applying global electric field (horizontally). Balancing of dual operation tuned an event occurring in a quantum well (2nm^2) wherein probability of transition between conformational states of a xanthene dye became function of local and global bias. A single xanthene dye *RB* in a quantum well showed gaussian probabilistic distribution of transition to different conformations. The bandwidth of Q band of gaussian distribution was tuned by horizontal bias to a maximum of 25% which revealed that it is possible to control local even globally which is basic requirement of this processor. And the tunable data we obtain are the processing information which is simulated by software to find logic in tuning. Thus it performs as most basic processor as described above.

[Meaning of symbol]

[0058]

101: One processing surface unit
102: Vertical electrode array unit
103: vertical electrodes
104: horizontal electrodes
107: neurons
402: Processing surface and source connecting interface
405: Output surface and motor connecting interface
501: Energy minima for one conducting state of neuron.
508: Multilevel response.
802: Electric field distribution on processing surface.
904: nth state neuron occupies allowed well.

1607: STM/AFM scanned complete solution surface
1613: Selective solution surface.
1901: ROM processor
1902: RAM processor
The others: see text

【書類名】　　外国語特許請求の範囲

1. A vertical parallel processor comprising a coupled template, wherein plural input signals are given horizontally from all directions on a surface situated in the middle of surrounding electrodes where the surface contains multilevel systems or neurons and output signals are taken vertically at different points on that surface.

2. The vertical parallel processor of **claim 1**, wherein plural input signals are given horizontally p×q from all directions on a square or rectangular surface situated in the middle of surrounding p+q+p+q electrodes where the surface contains multilevel systems or neurons and m×n dimensional output signal are taken vertically at different points on that surface.

Here the value of *m, n, p, q* are numbers varying from 0 to infinity, but both *m* and *n*, or both *p* and *q* cannot be zero simultaneously.

3. The vertical parallel processor of **claim 1**, wherein plural input signals are given horizontally from all directions on a triangular, circular or polygonal surface situated in the middle of surrounding electrodes where the surface contains multilevel systems or neurons and output signals are taken vertically at different points on that surface.

4. The vertical parallel processor of any one of **claim 1-3,** wherein the template surface is conducting and vertical electrodes measure STM based tunneling current through multilevel systems or neurons.

5. The vertical parallel processor of any one of **claim 1-3,** wherein the template surface is conducting and vertical electrodes measure AFM based atomic force to come into contact with the multilevel systems or neurons.

6. The vertical parallel processor of any one of **claim 1-5** with thin films on processing surface comprising materials having redox active center or conformational sensitive center, containing at least two of the following properties A, B and C

A. Materials incorporated between pair of electrodes show stable multilevel conductivity at any particular bias in a definite range or application.

B. Each state could be induced by applying different bias conditions.

C. Transient current response to rectangular voltage pulse is an evoluted form of gaussian, or step or ramp or staircase one.

7. The vertical parallel processor of any one of **claim 1-6,** wherein multilevel system or neurons comprising A, B, C or D.

A. Sensor for specific signal detection and real world signals like sound, heat, light and any other form of energy when falls on the surface specifically designed sensor converts the signal into a 1D array of electronic signals;

B. Small processing unit of any other functional materials of specific function resulting in conversion of whole processing surface into different regions with different functionality;

C. Multilevel systems or neurons that can reversibly switch between all possible conducting states and remember the state more than the time of reaching equilibrium for whole surface (RAM) and refreshed as many times;

D. multilevel systems or neurons which once switch to one of the possible multilevel states remains permanently in the same state (ROM).

8. The vertical parallel processor of any one of **claim 1-7,** wherein vertical electrodes are nanoscale width and macroscale length structure of similar heights with atomic edged tip where number of tips in one electrode system comprising A or B.

A. One atomic edge to consider one solution point is single atomic edge tip,

B. Defined number of atomic edges in single electrode unit wherein solution point is average response of collective output for all individual atomic edges.

9. The vertical parallel processor of any one of **claim 1-8,** wherein inputs are connected to neural node controller where all input signals are divided parallely into different unit preceding the processor and switching between each unit containing A, B, C, D or E.

A. Unit that could vary the sequence order and intermediate ground connections;

B. Unit that permute the same arrayed input is into differently ordered array

C. Unit that passes arrayed input parallely through processor of different geometry to generate coupled output.

D. Unit that replace some of the input by pulsed array source

E. Unit that passes input signals through channels where signals are multiplied or divided to match with input impedance of whole processing surface.

10. The vertical parallel processor of any one of **claim 1-9,** wherein number of ground connection for p×q inputs varies 1 to pq-1 to process same set of arrayed input; each combination of grounds generates a specific node of operation and each node have their own neural network so that after training and developing rules these nodes are used in different situations where a special kind of processing is required.

11. A vertical parallel processor comprising a coupled template, wherein plural input is given vertically from top on a horizontal surface situated in the middle of surrounding electrodes where the surface containing multilevel systems or neurons and output signals are taken horizontally through the electrodes.

12. The vertical parallel processor of **claim 11**, wherein vertical plural input electrodes have flat or spherical front edge generating local bias over large area on the processing surface; front edge area of vertical electrodes containing(or composing) A, B, and C

A. Total area, which is sum of all individual vertical electrodes, cover more than a definite percentage of processing surface; wherefrom we generate nodes of input operations for every class of operations.

B. Relative area of electrode bundle or individual vertical electrode varied tuning control of individual input on final solution surface.

C. Front edge geometry modified to tune potential distribution of the contours on processing surface.

13. A cluster which comprises
vertical parallel processors of any one of claim 1-8;
neural node controller; and
connections motors sensors connected following ways A, B and C.

A. Some or all of the processors input connected to an array of vertical processors, rest of them to output of sensors which are free input of the whole system;

B. Some of its output connected to some of the output motors and rest of them connected to other vertical processors;

C. All free outputs connected to motors and not connected to any input of the whole system, taken vertically as a final cluster output.

14. (Model claim). A modified virtual source neural network model which comprises the vertical parallel processor of any one of claim 1-13, and its modification contains A, B and C.

A. Binary neuron (having value 0 or 1) or continuum neurons (any value 0 to 1) of old concepts is replaced by multilevel system or neurons (selected values between 0 to 1).

B. Introduction of virtual sources as effective input to each neuron does not come from other neurons.

C. Modification is accession to individual outputs as we take output vertically; hence model becomes a 3D (3 dimensional) model.

15. The modified virtual source neural network model of **claim 14** whose configuration is developed by minimization of an energy term containing vector sum of the products of weight generated by effective inputs from virtual sources or global weightage and vertical probe generated weight or local weightage and these two positive contribution are negated with weightage generated by the threshold value of multilevel states.

16. The modified virtual source neural network model of **claim 14** or **15** containing A, B, and/or C.

A. feed-forward network by connecting some or all output of the vertical parallel processor model back to its own input directly or indirectly;

B. model with one or more hidden layers of multilevel neurons and generating lower or equal number of output at different levels to reach final output;

C. intermediate layers composed of mixed multilevel logic neurons, which comprise more than one kind of logical neurons together like tetranary or octanary systems or other logical systems.

17. A processor training method to train single vertical parallel processor of any one of claim 1-13 where input and output are correlated by artificial neural network model of claim 14-16 finding rule or weight coefficients of virtual neurons or multilevel systems following major initialization of the below training steps (1)-(3).

(1) Firstly finding range of application for local bias and global bias;
(2) secondly finding their levels of operations or functional behavior for each multilevel logic states;
(3) finally developing logical function by energy minimization so that when an unpredictable input is given it can give most probable solution of the problem.

18. The processor training method of **claim 17**, wherein developing logical function in above step (3) for performing mathematical operations, comprises A or B addressing functional criteria containing C or D.

A. Via concept of matrix inversion process, where 3D matrix inversion to linearized array for vertical input horizontal output of any one of **claim 1-10.**

B. Via linearized array to 3D matrix conversion for horizontal input and vertical output; which is basic operation method for the processor of **claim 11 or 12**.

C. probe bias is used as operator to treat mathematical functions.

D. ground connection variation of **claim 10** with geometrical processing surface variation of any one of **claim 1-3, 11, and 12** is used to generate specific functional criteria.

19. The processor training method of **claim 17** for clusters of claim 13 wherein training is done following model described in **claim 14-16** containing basic considerations A, B, and C.

A. Input of the processor is free input of the cluster considered as 2D input array, output of the processor is final output of the cluster considered as 3D array and all basic processor components of cluster is replaced by one or more layer of multilevel neurons.

B. Individual components of the cluster are trained first and then its importance in final output is determined by finding functional relationship with most similar part in final output pattern.

C. As there are two different kinds of inputs in clusters, directly from sensors or from any other processors hence importance of two different kinds of inputs to the final pattern is determined by finding functional relationship.

20. The processor training method of **claim 17** for processors of **claim 11 or 12** comprising steps A, B and C

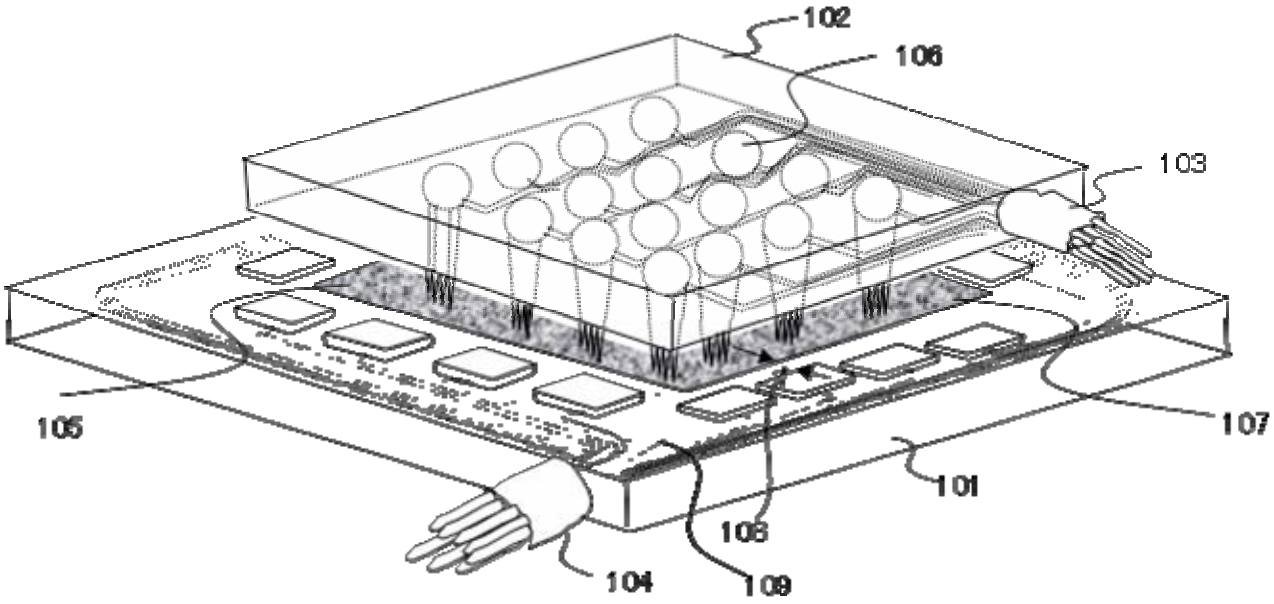
A. finding range of application for local bias and global bias with additional criteria of crosschecking reproducibility of neurons in the contour on processing surface generated by field projection from vertical electrodes.

B. finding functional behavior for transition to each multilevel state along with field distribution contour generated by interplaying of neighboring vertical electrodes.

C. developing logical function by energy minimization considering minimum energy path from one horizontal electrode to another.

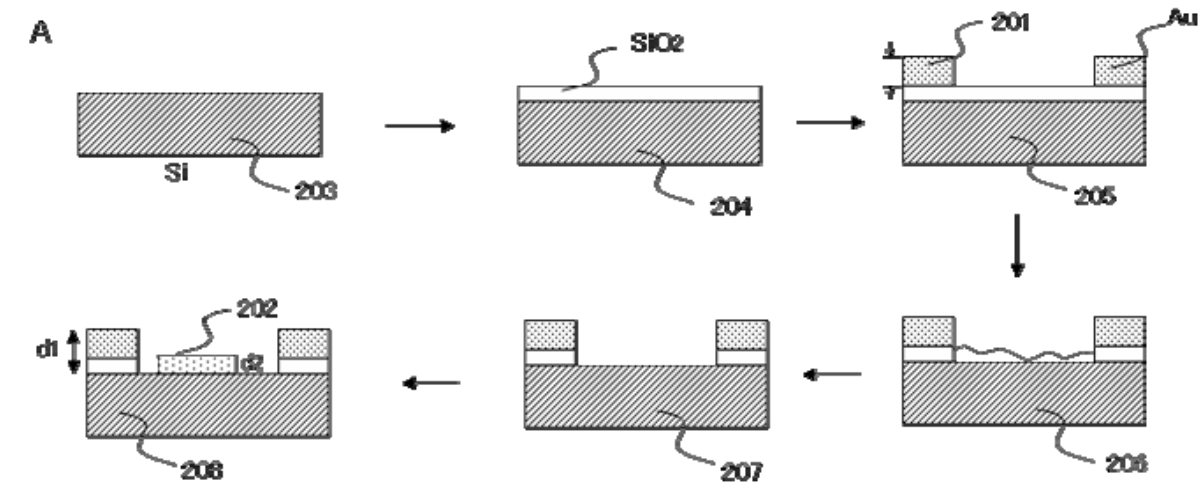
【書類名】　　図面
【図１】

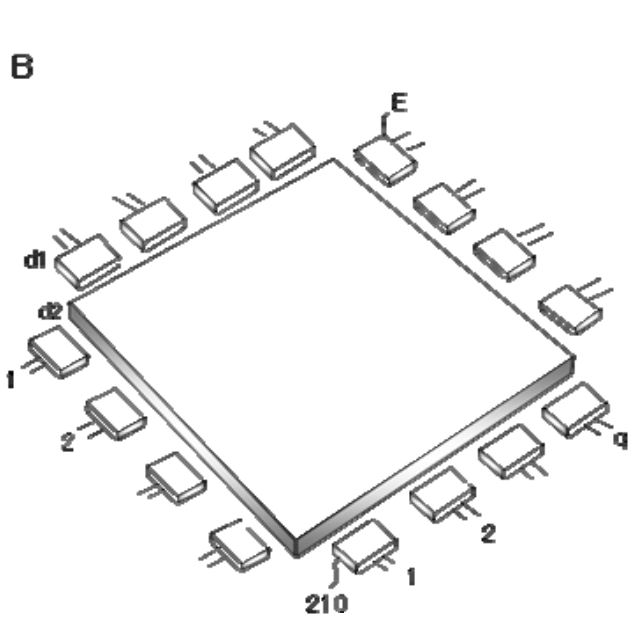
Fig1

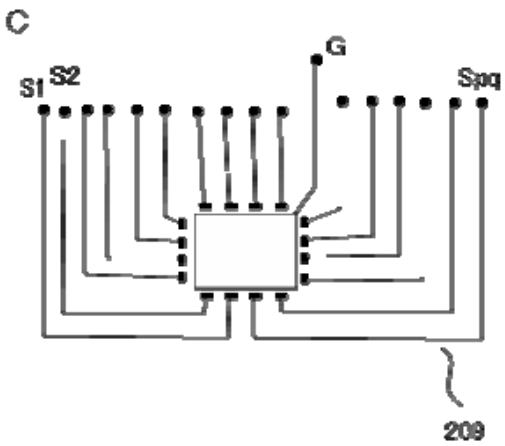


【図２】

Fig 2

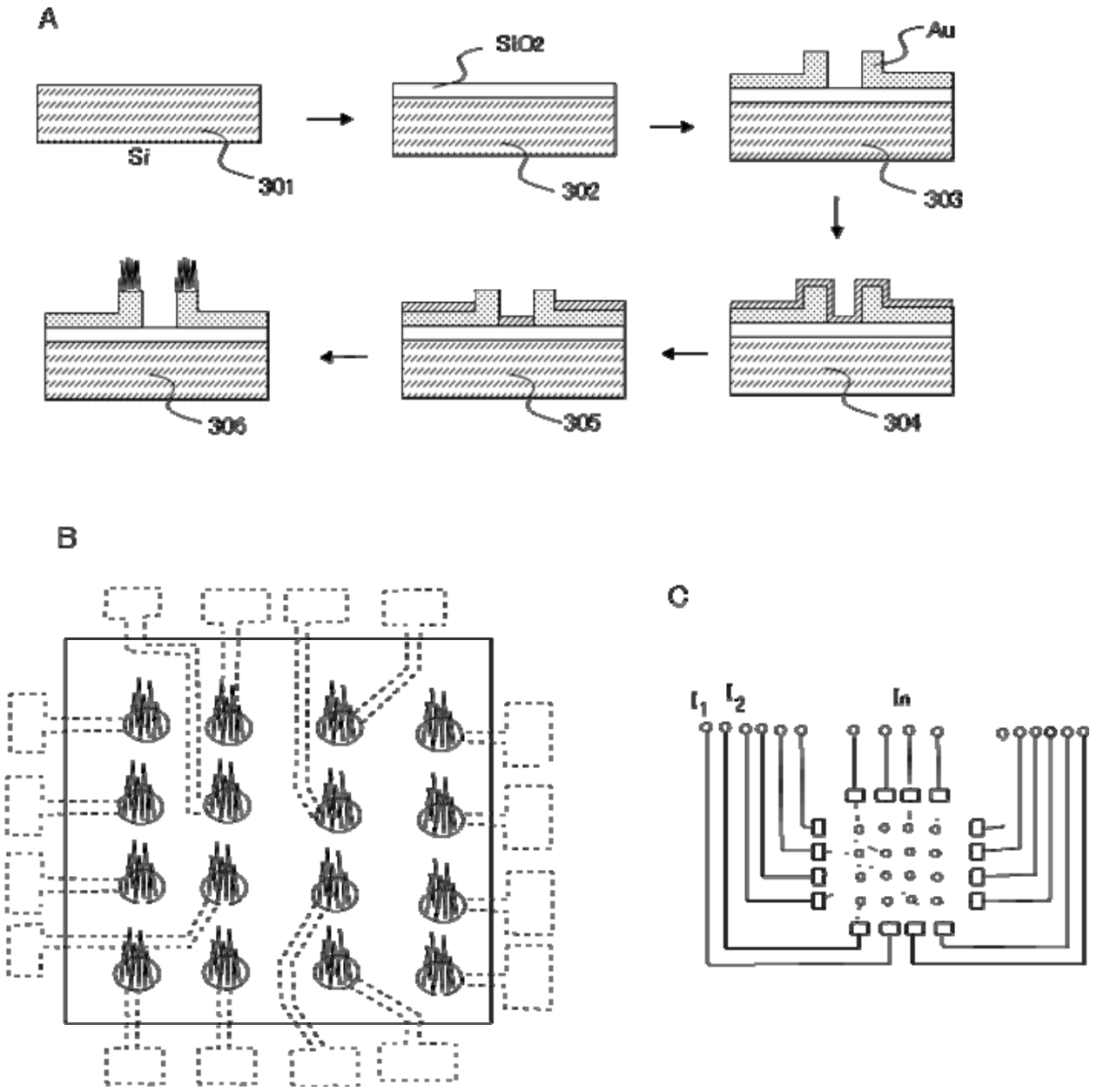

A
Si
203
SiO2
204
201
Au
205
206
207
202
d1
d2
208


B
E
d1
d2
1
2
q
2
1
210


C
G
S1
S2
Spq
209

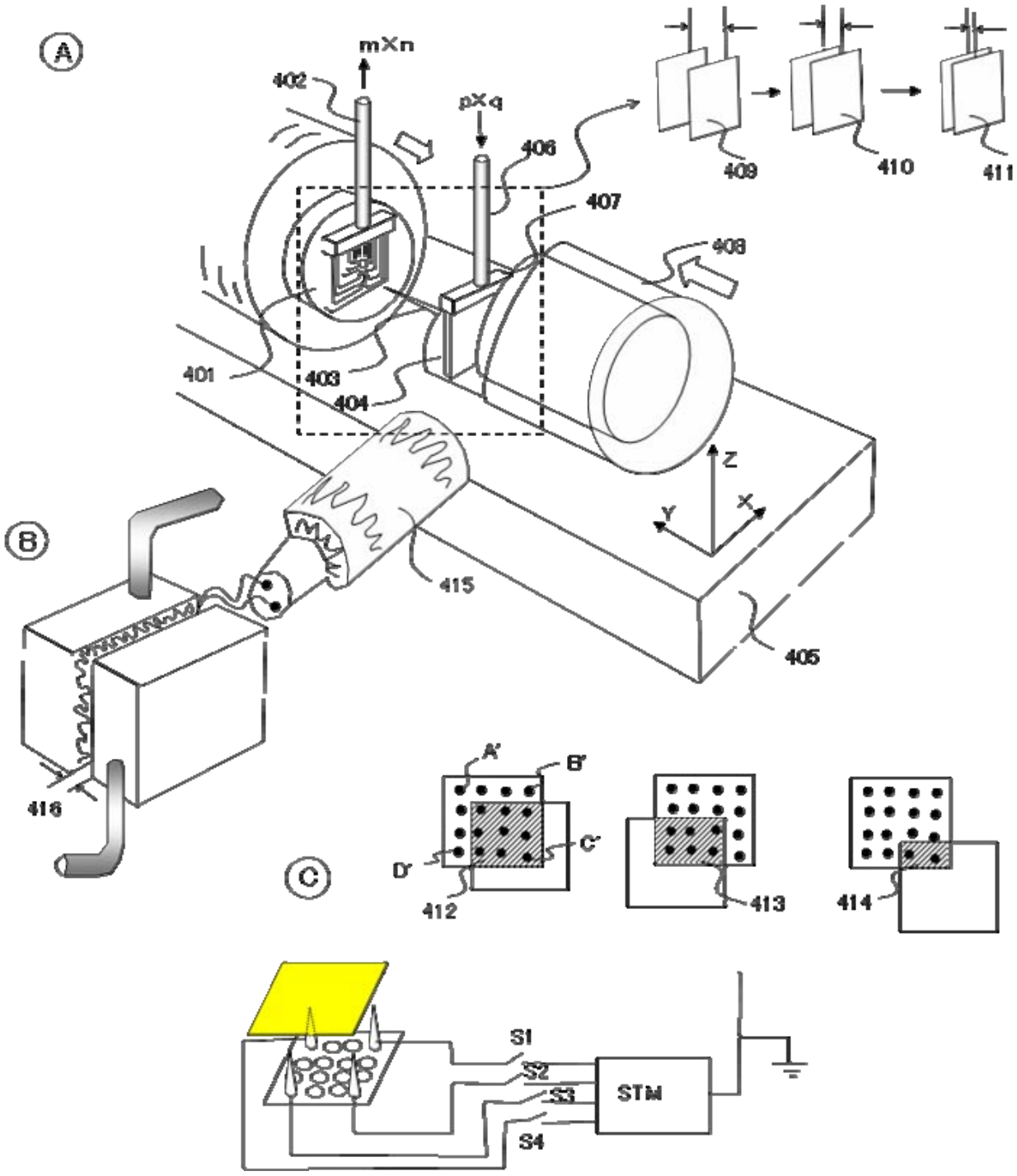
【図３】

Fig 3



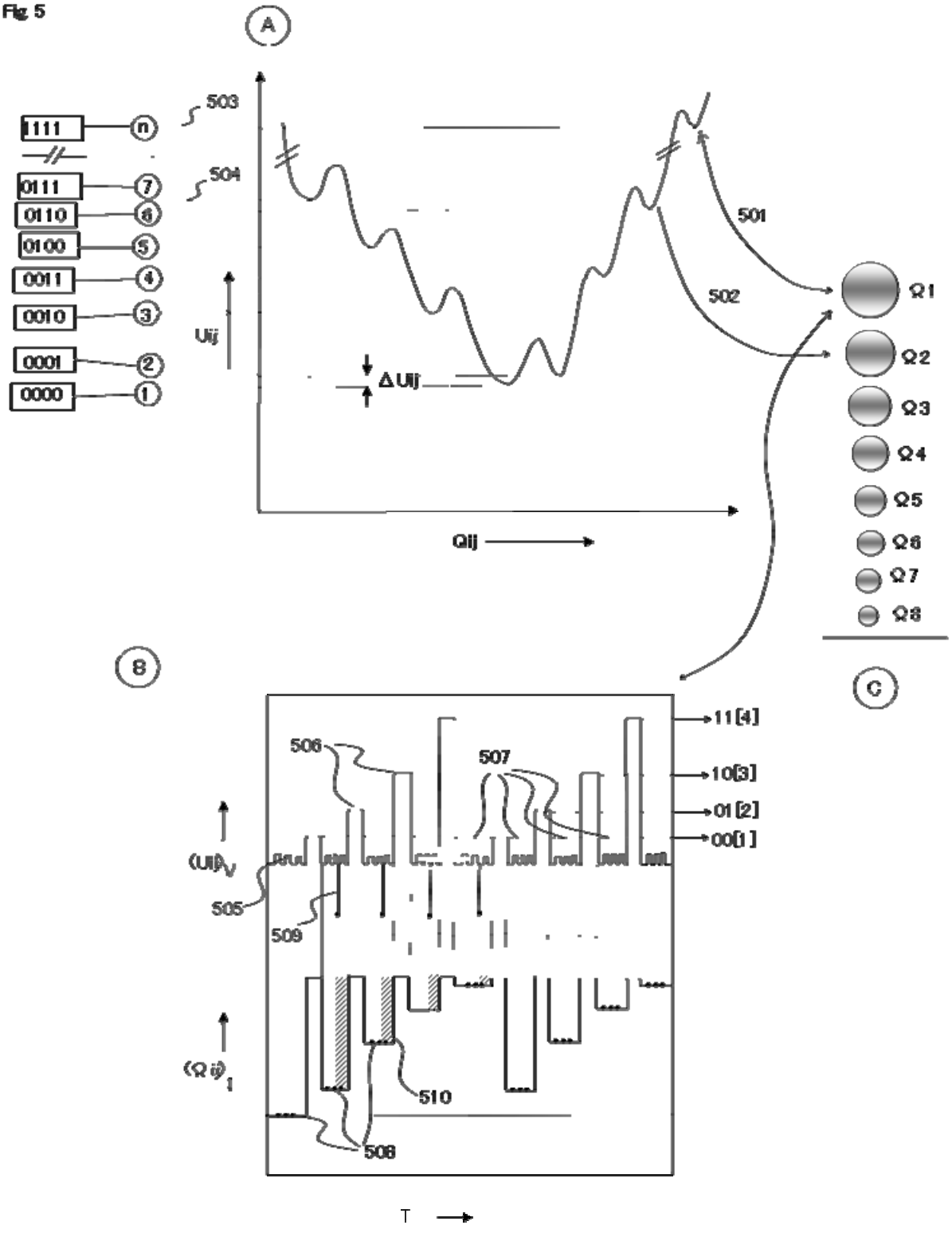
【図４】

Fig. 4


A
mXn
402
pXq
406
407
408
409
410
411
401
403
404
Z
Y
X
B
415
405
416
C
A'
B'
C'
D'
412
413
414
S1
S2
S3
S4
STM

【図５】

Fig 5


A
1111
n
0111
7
0110
6
0100
5
0011
4
0010
3
0001
2
0000
1
503
504
Uij
ΔUij
Qij
501
502
Ω1
Ω2
Ω3
Ω4
Ω5
Ω6
Ω7
Ω8
C
B
11[4]
10[3]
01[2]
00[1]
506
507
505
509
510
508
T

【図６】

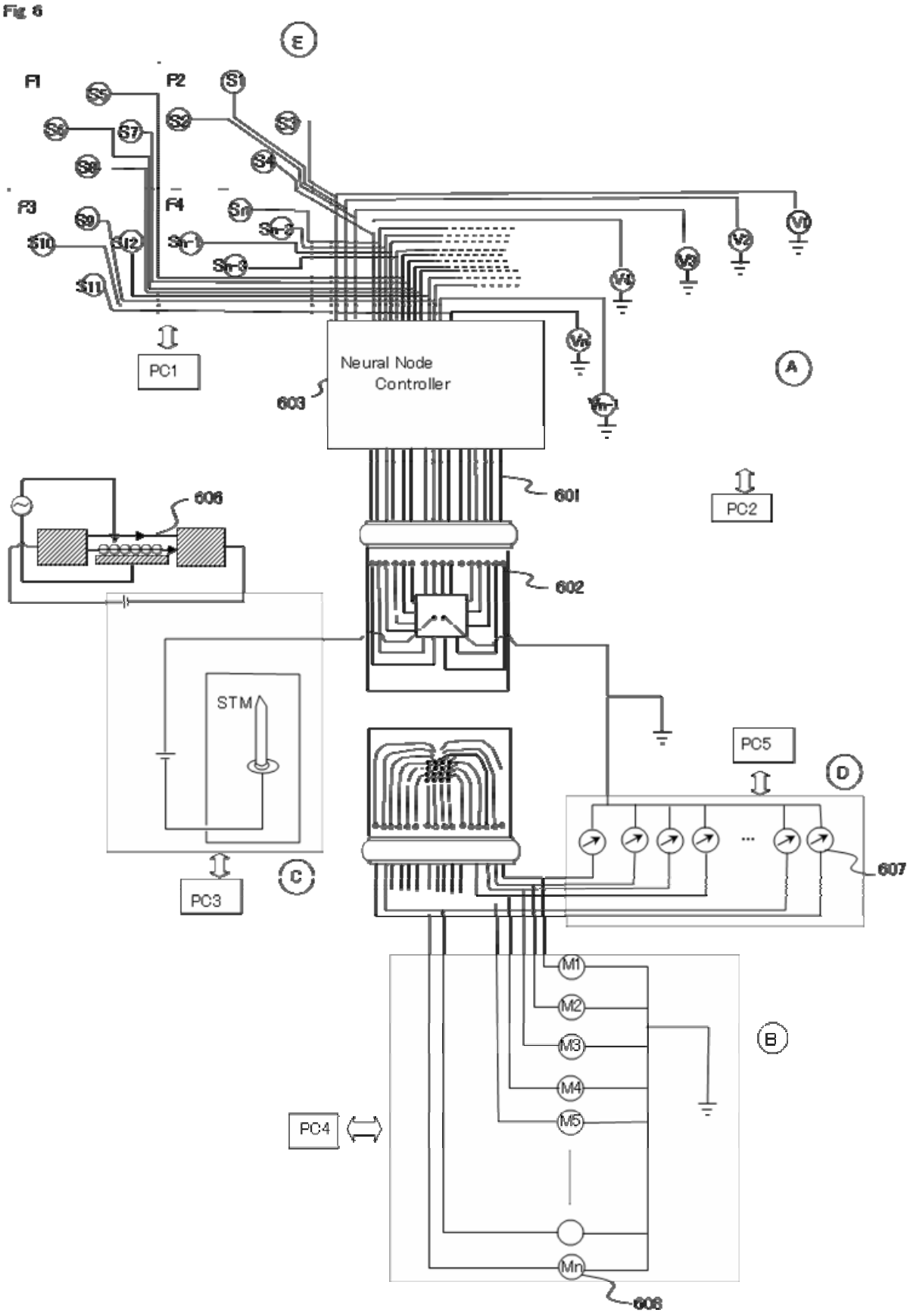
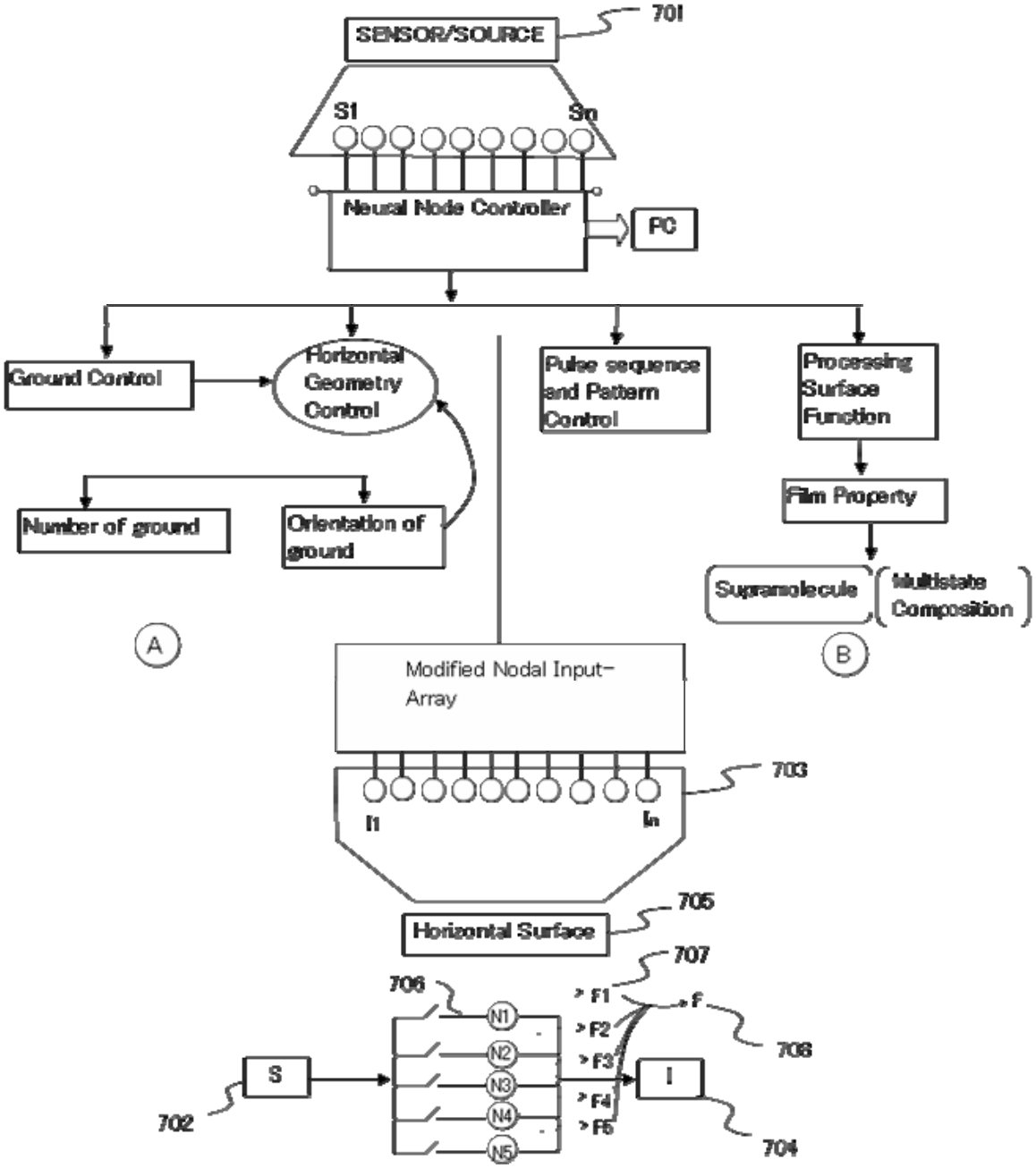


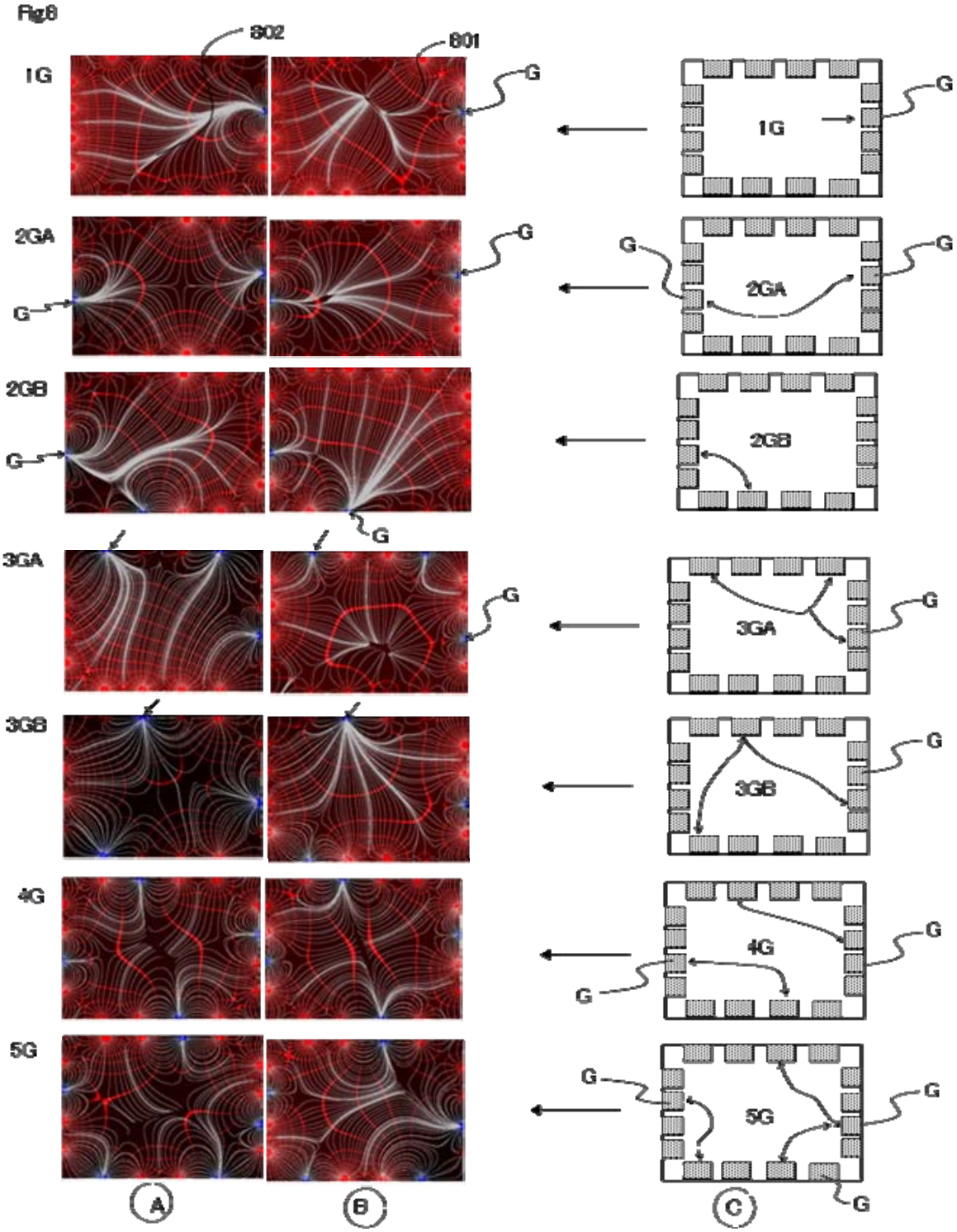
Fig 6
E
F1
F2
F3
F4
PC1
Neural Node
Controller
603
A
601
PC2
606
602
STM
PC5
D
607
C
PC3
M1
M2
M3
M4
M5
Mn
B
PC4
608

【図７】

Fig 7

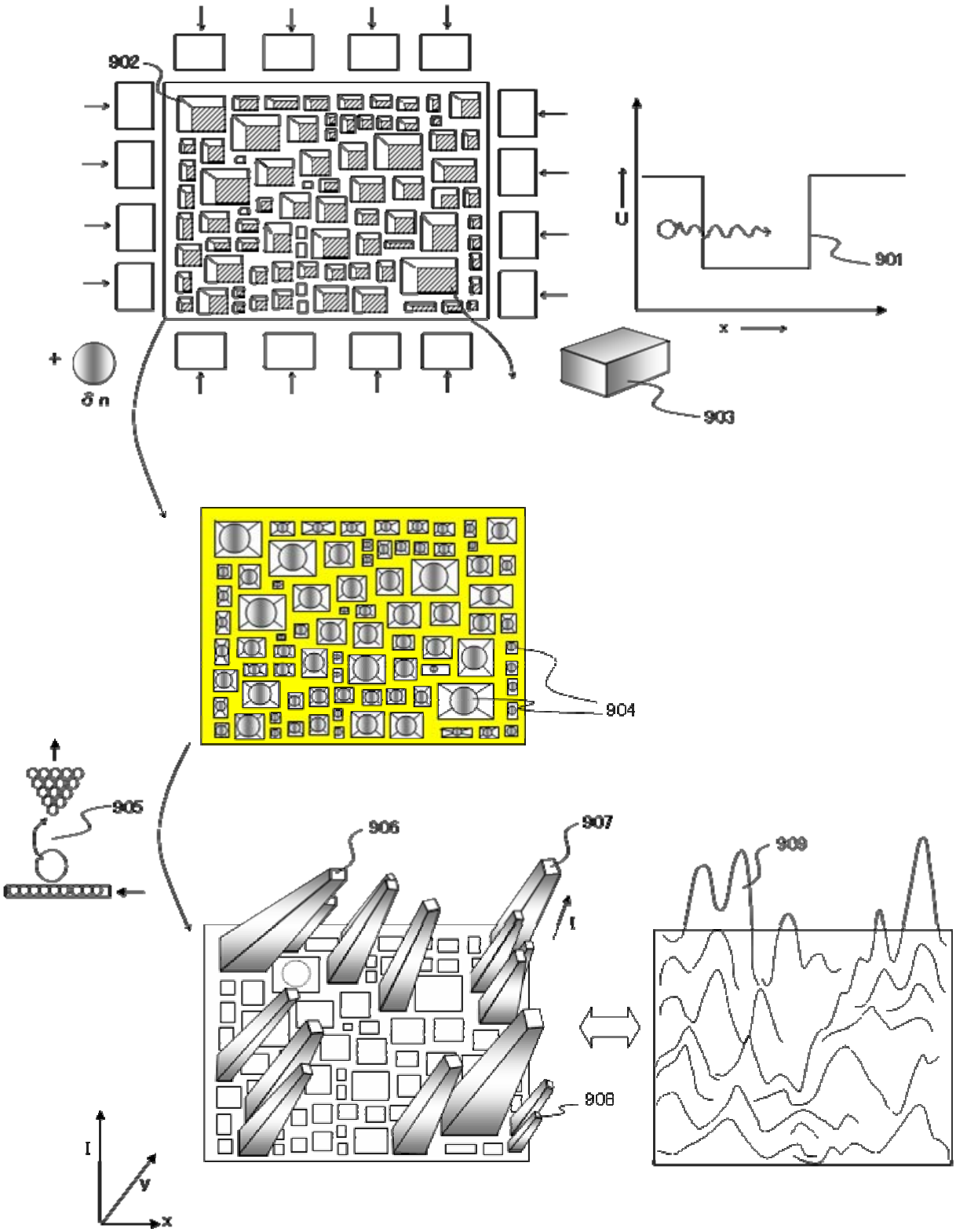

701
SENSOR/SOURCE
S1
Sn
Neural Node Controller
PC
Ground Control
Horizontal Geometry Control
Number of ground
Orientation of ground
Pulse sequence and Pattern Control
Processing Surface Function
Film Property
Supramolecule
Multistate Composition
A
B
Modified Nodal Input-Array
703
I1
In
705
Horizontal Surface
707
706
F1
F2
F3
F4
F5
F
708
N1
N2
N3
N4
N5
S
I
702
704

【図８】



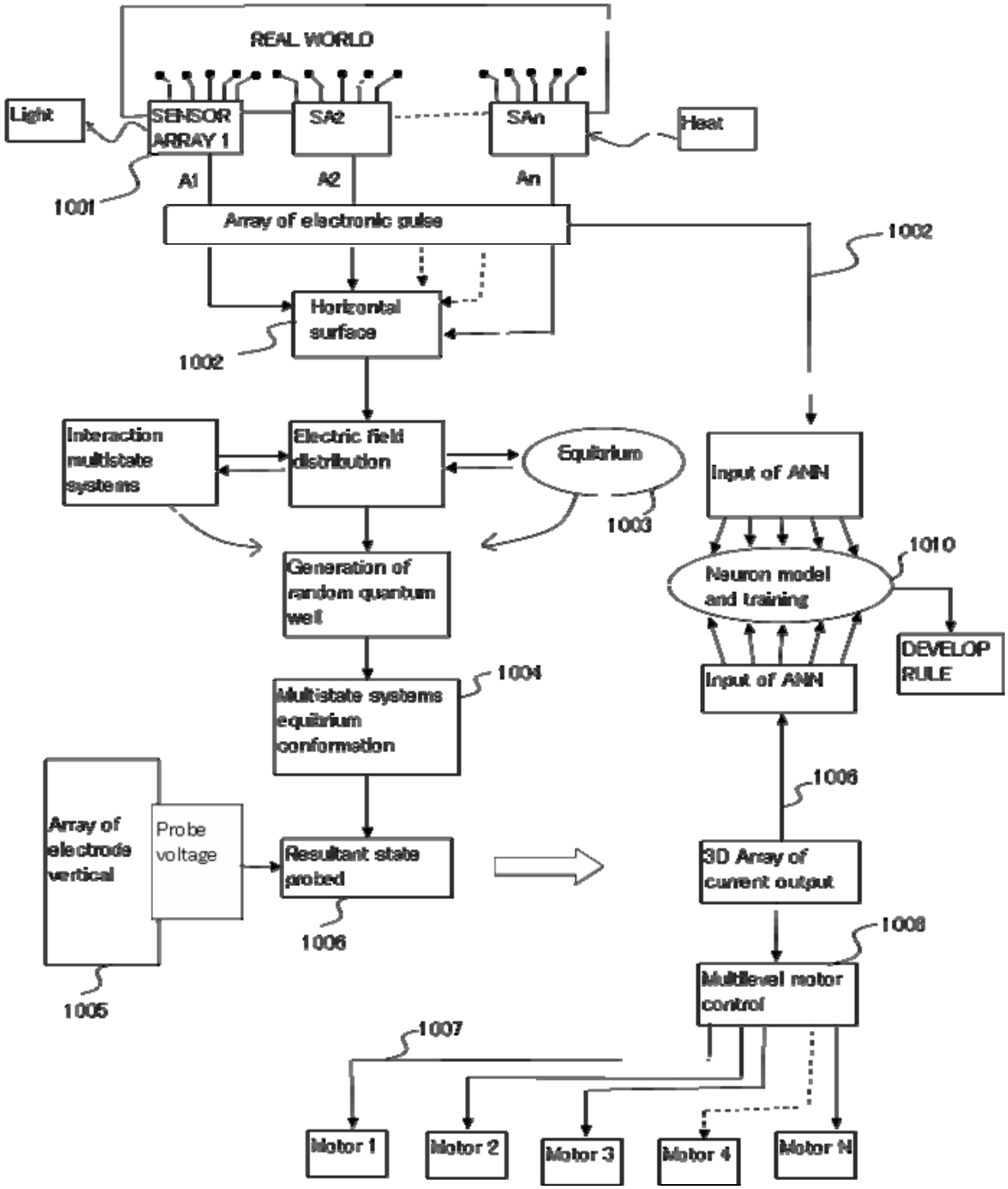
【図９】

Fig9



【図１０】

Fig10


REAL WORLD
Light
SENSOR ARRAY 1
SA2
SAn
Heat
A1
A2
An
1001
Array of electronic pulse
1002
Horizontal surface
1002
Interaction multistate systems
Electric field distribution
Equilirium
1003
Input of ANN
Generation of random quantum well
Neuron model and training
1010
DEVELOP RULE
Input of ANN
Multistate systems equilirium conformation
1004
1006
Array of electrode vertical
Probe voltage
Resultant state probed
1006
3D Array of current output
1008
Multilevel motor control
1005
1007
Motor 1
Motor 2
Motor 3
Motor 4
Motor N

【図１１】

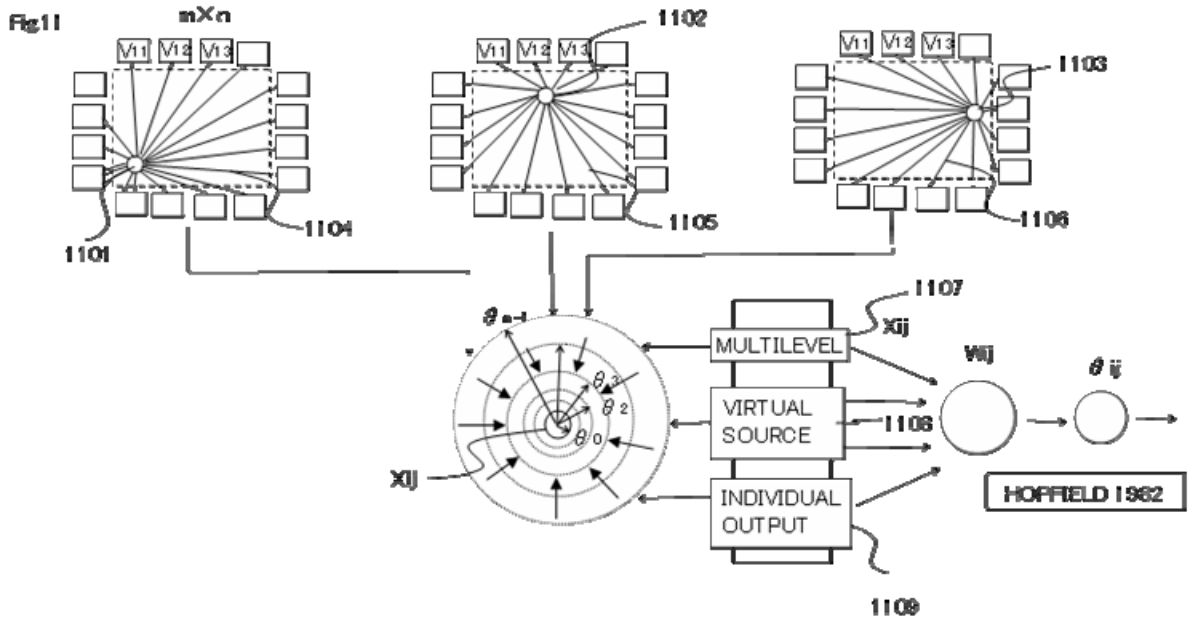
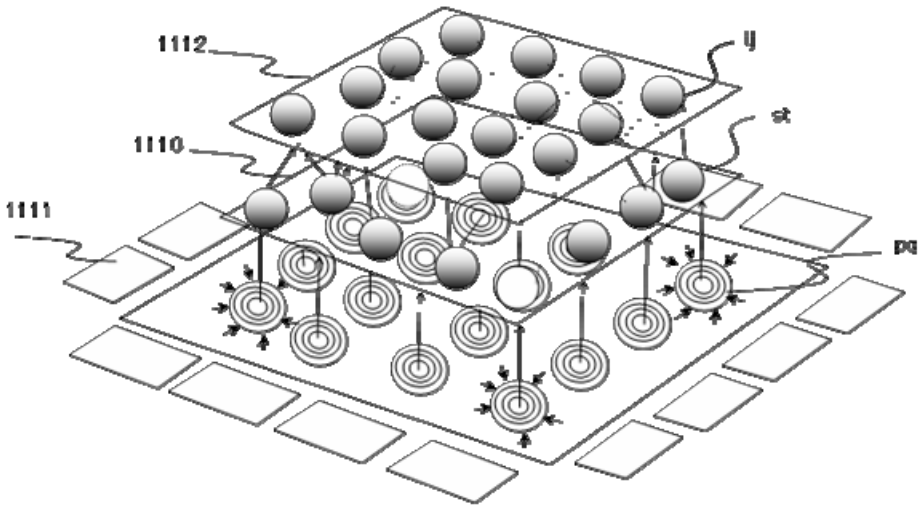
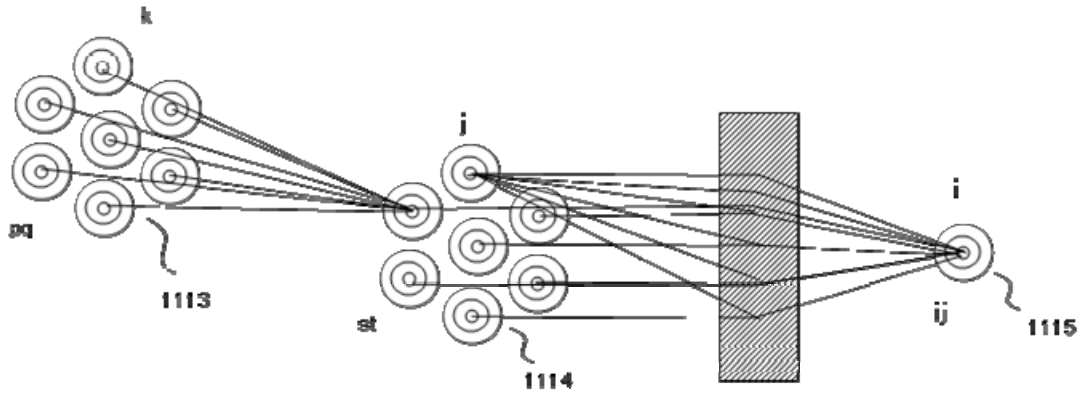


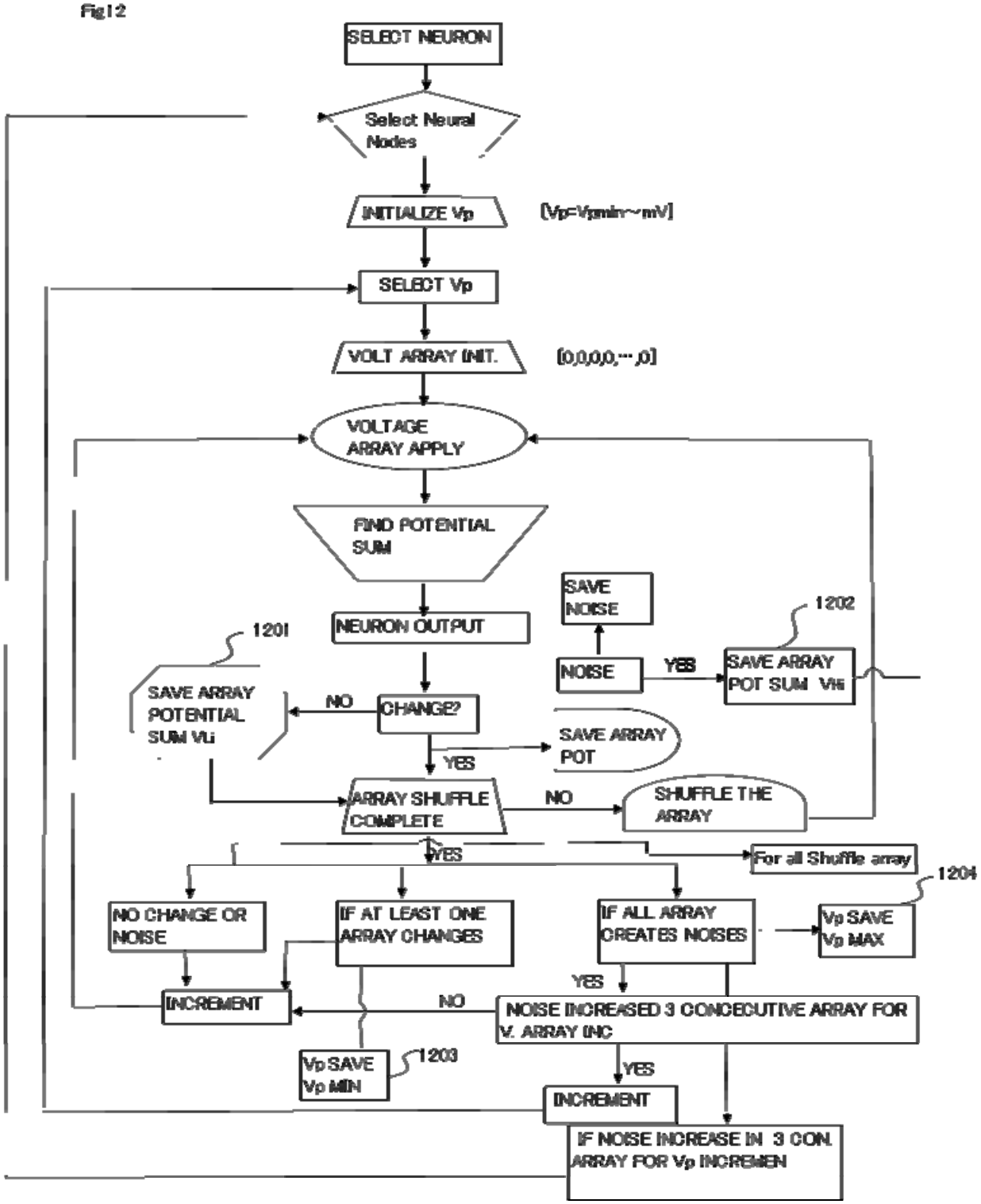
Fig11
mXn
V11
V12
V13
1101
1102
1103
1104
1105
1106
1107
Xij
MULTILEVEL
VIRTUAL SOURCE
INDIVIDUAL OUTPUT
1108
1109
Vij
θ ij
HOPFIELD 1982


1112
1110
1111
ij
st
pq


k
pq
1113
j
st
1114
i
ij
1115

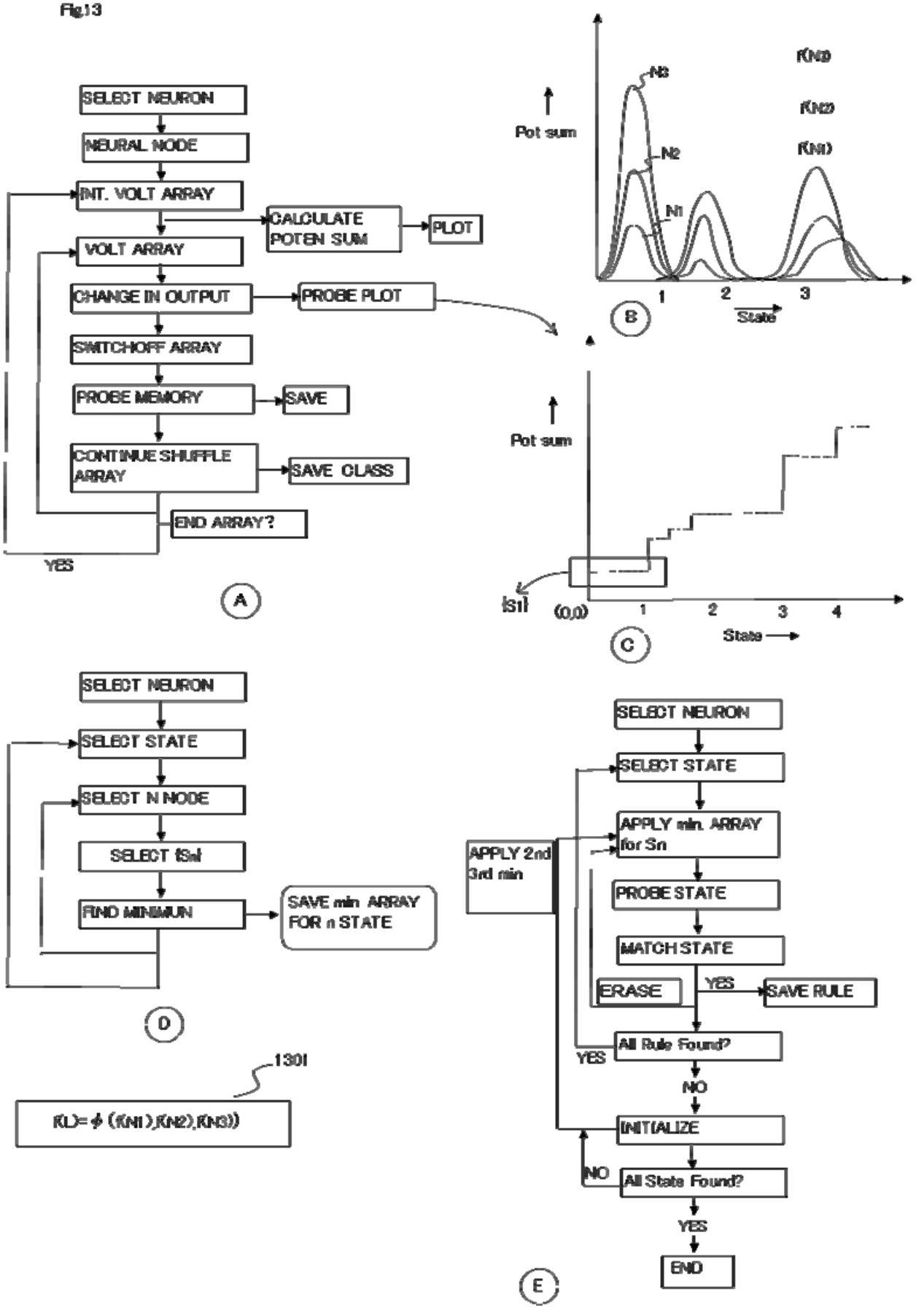
【図１２】

Fig12


SELECT NEURON
Select Neural Nodes
INITIALIZE Vp
[Vp=Vpmin~mV]
SELECT Vp
VOLT ARRAY INIT.
[0,0,0,0,…,0]
VOLTAGE ARRAY APPLY
FIND POTENTIAL SUM
NEURON OUTPUT
1201
SAVE ARRAY POTENTIAL SUM Vti
NO
CHANGE?
YES
SAVE ARRAY POT
SAVE NOISE
1202
NOISE
YES
SAVE ARRAY POT SUM Vti
ARRAY SHUFFLE COMPLETE
NO
SHUFFLE THE ARRAY
YES
For all Shuffle array
1204
NO CHANGE OR NOISE
IF AT LEAST ONE ARRAY CHANGES
IF ALL ARRAY CREATES NOISES
Vp SAVE Vp MAX
YES
INCREMENT
NO
NOISE INCREASED 3 CONCECUTIVE ARRAY FOR V. ARRAY INC
Vp SAVE Vp MIN
1203
YES
INCREMENT
IF NOISE INCREASE IN 3 CON. ARRAY FOR Vp INCREMEN

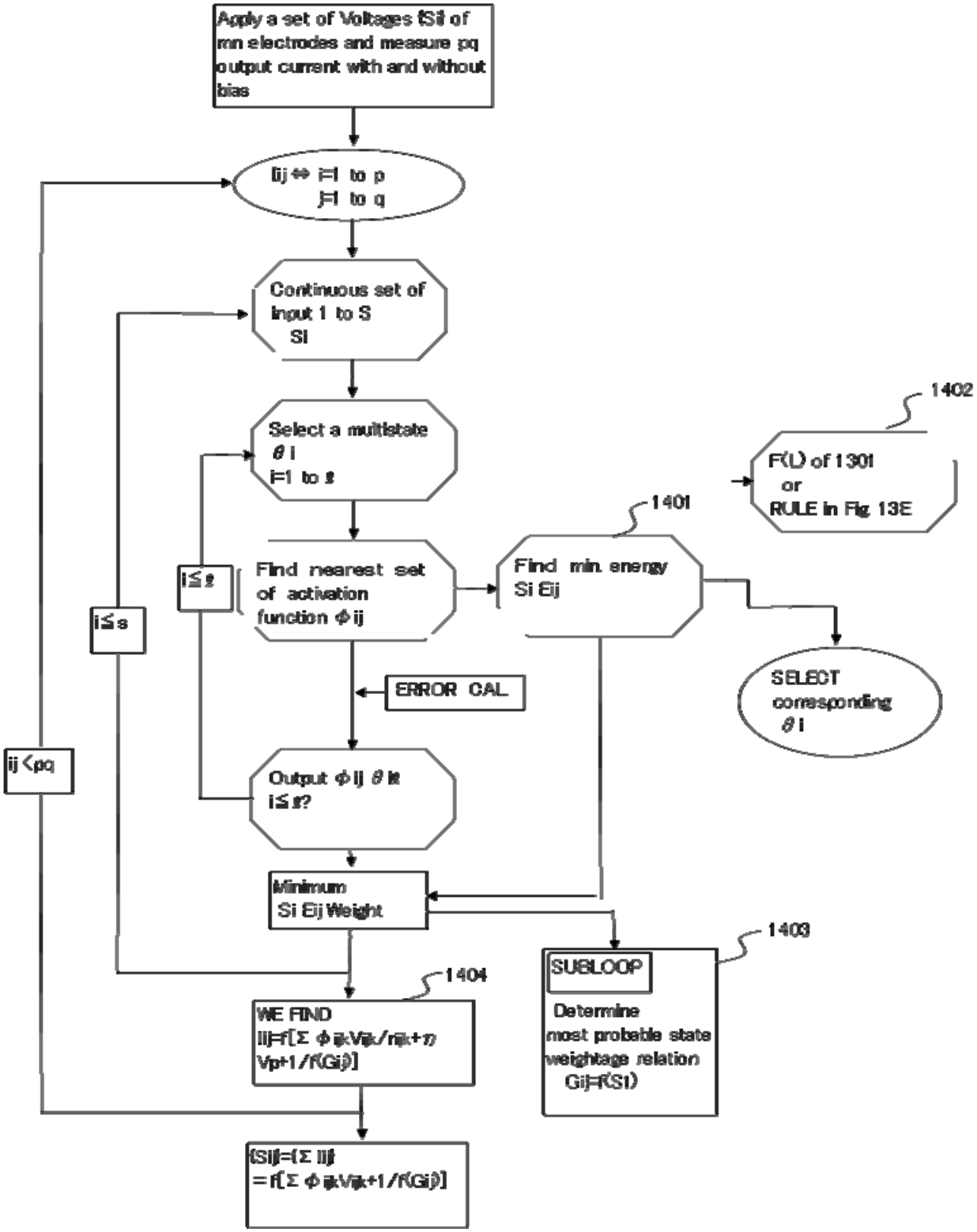
【図１３】

Fig.13


SELECT NEURON
NEURAL NODE
INT. VOLT ARRAY
CALCULATE POTEN SUM
PLOT
VOLT ARRAY
CHANGE IN OUTPUT
PROBE PLOT
SWITCHOFF ARRAY
PROBE MEMORY
SAVE
CONTINUE SHUFFLE ARRAY
SAVE CLASS
END ARRAY?
YES
A
Pot sum
N3
N2
N1
f(N3)
f(N2)
f(N1)
1
2
3
State
B
Pot sum
|Si|
(0,0)
1
2
3
4
State
C
SELECT NEURON
SELECT STATE
SELECT N NODE
SELECT |Si|
FIND MINIMUN
SAVE min ARRAY FOR n STATE
D
1301
f(L)= ϕ (f(N1),f(N2),f(N3))
SELECT NEURON
SELECT STATE
APPLY min. ARRAY for Sn
APPLY 2nd 3rd min
PROBE STATE
MATCH STATE
ERASE
YES
SAVE RULE
All Rule Found?
YES
NO
INITIALIZE
NO
All State Found?
YES
END
E

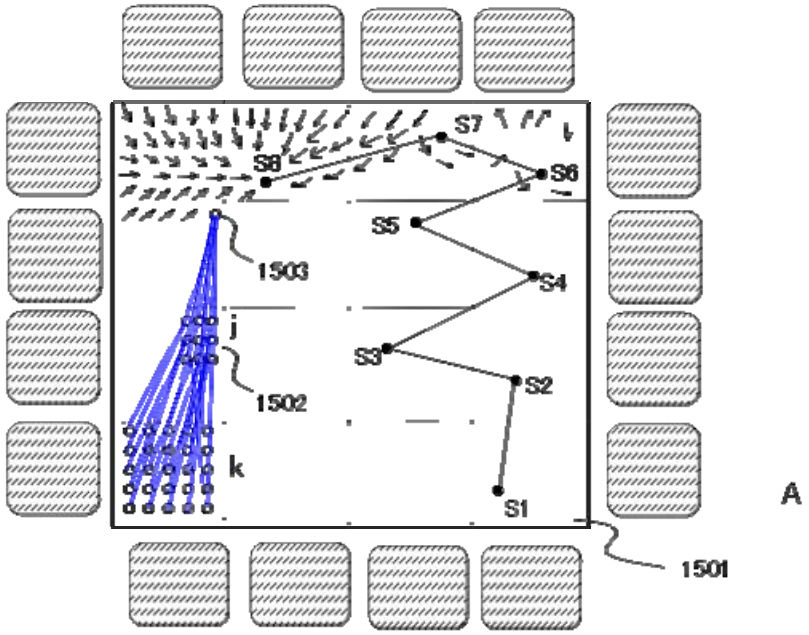
【図１４】

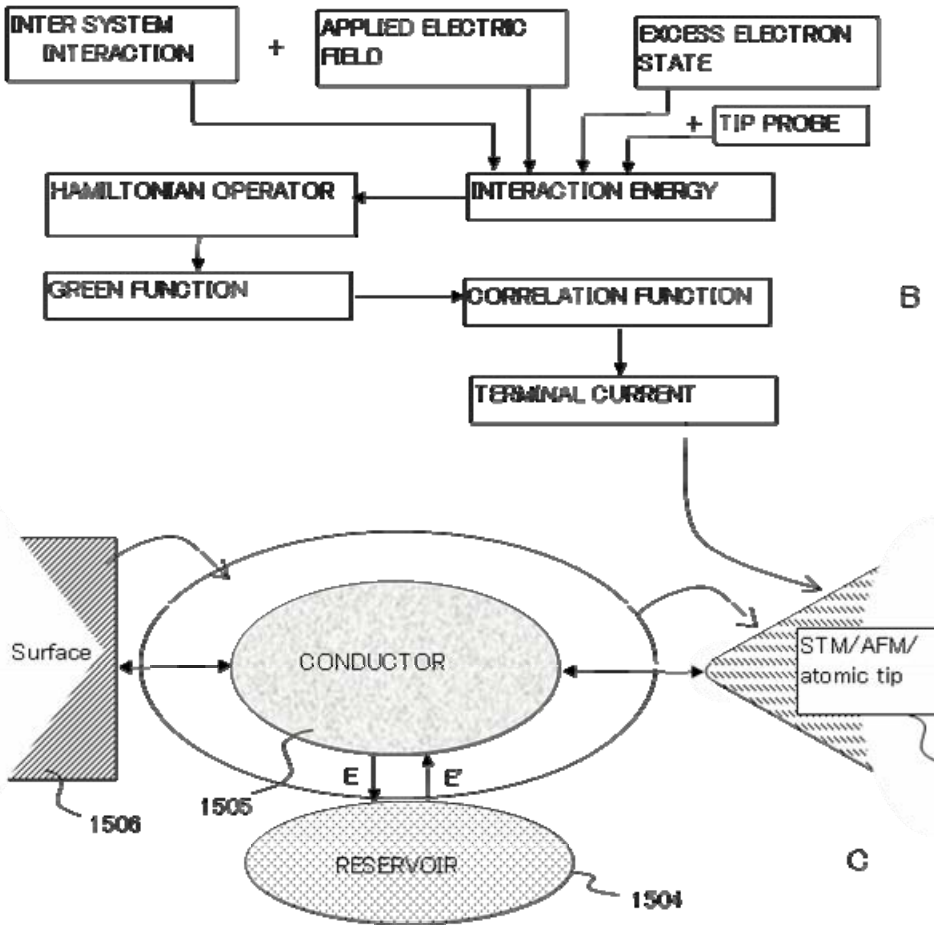
Fig14


Apply a set of Voltages {Si} of mn electrodes and measure pq output current with and without bias
Continuous set of Input 1 to S Si
Select a multistate θ l l=1 to s
Find nearest set of activation function φ ij
i≦s
i≦s
ERROR CAL
Output φ ij θ lt i≦s?
ij<pq
1401
Find min. energy Si Eij
1402
F(L) of 1301 or RULE in Fig 13E
SELECT corresponding θ l
Minimum Si Eij Weight
1403
SUBLOOP
Determine most probable state weightage relation Gij=F(Si)
1404
WE FIND
Iij=f[Σ φijkVjk/rijk+η
Vp+1/f(Gij)]
{Sij=(Σ Iij
=f[Σ φijkVjk+1/f(Gij)]

【図１５】

Fig15


S7
S8
S6
S5
S4
S3
S2
S1
1503
j
1502
k
1501
A


INTER SYSTEM INTERACTION
+
APPLIED ELECTRIC FIELD
EXCESS ELECTRON STATE
+ TIP PROBE
HAMILTONIAN OPERATOR
INTERACTION ENERGY
GREEN FUNCTION
CORRELATION FUNCTION
B
TERMINAL CURRENT
Surface
CONDUCTOR
STM/AFM/
atomic tip
E
E'
1505
1506
RESERVOIR
1504
C

【図１６】

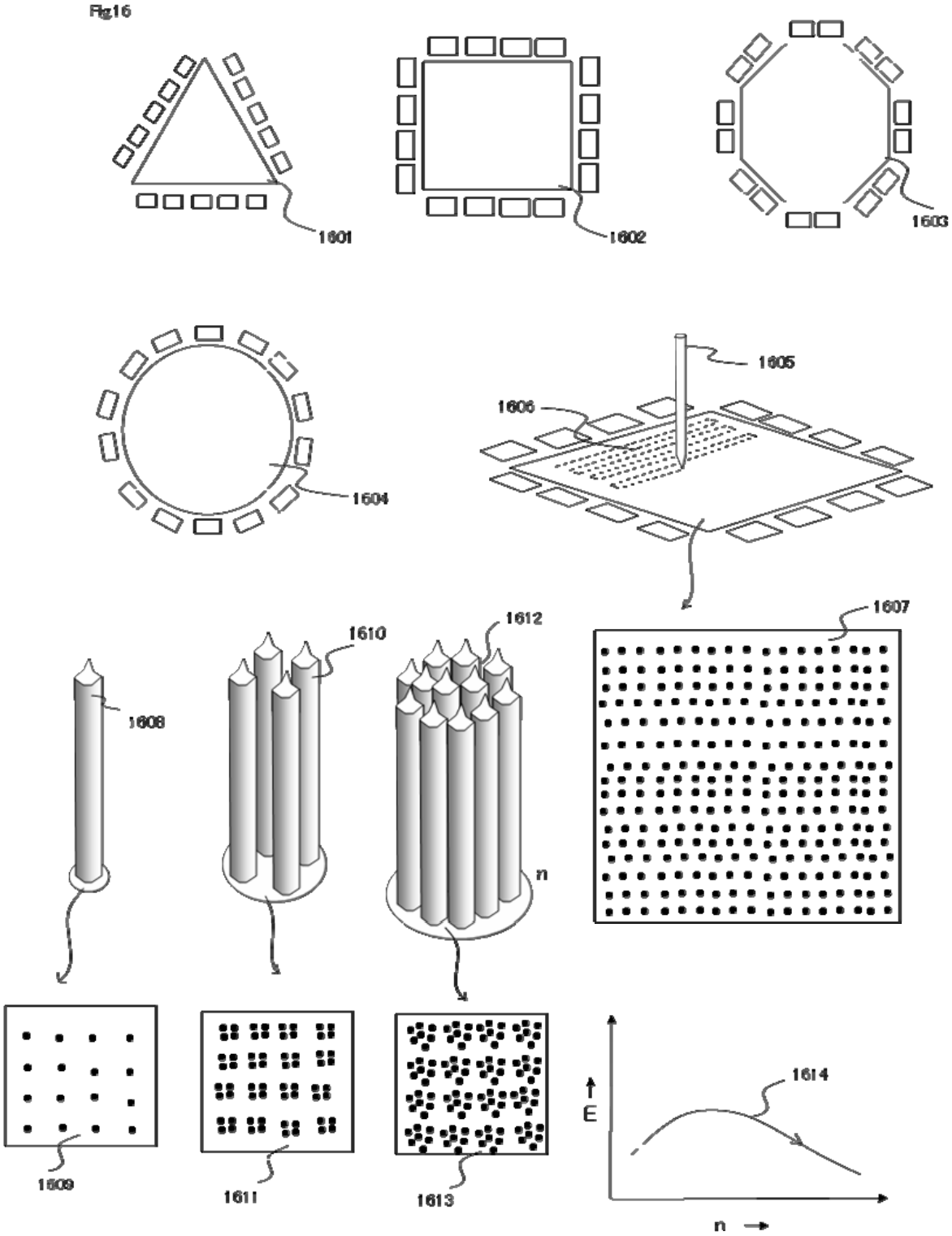
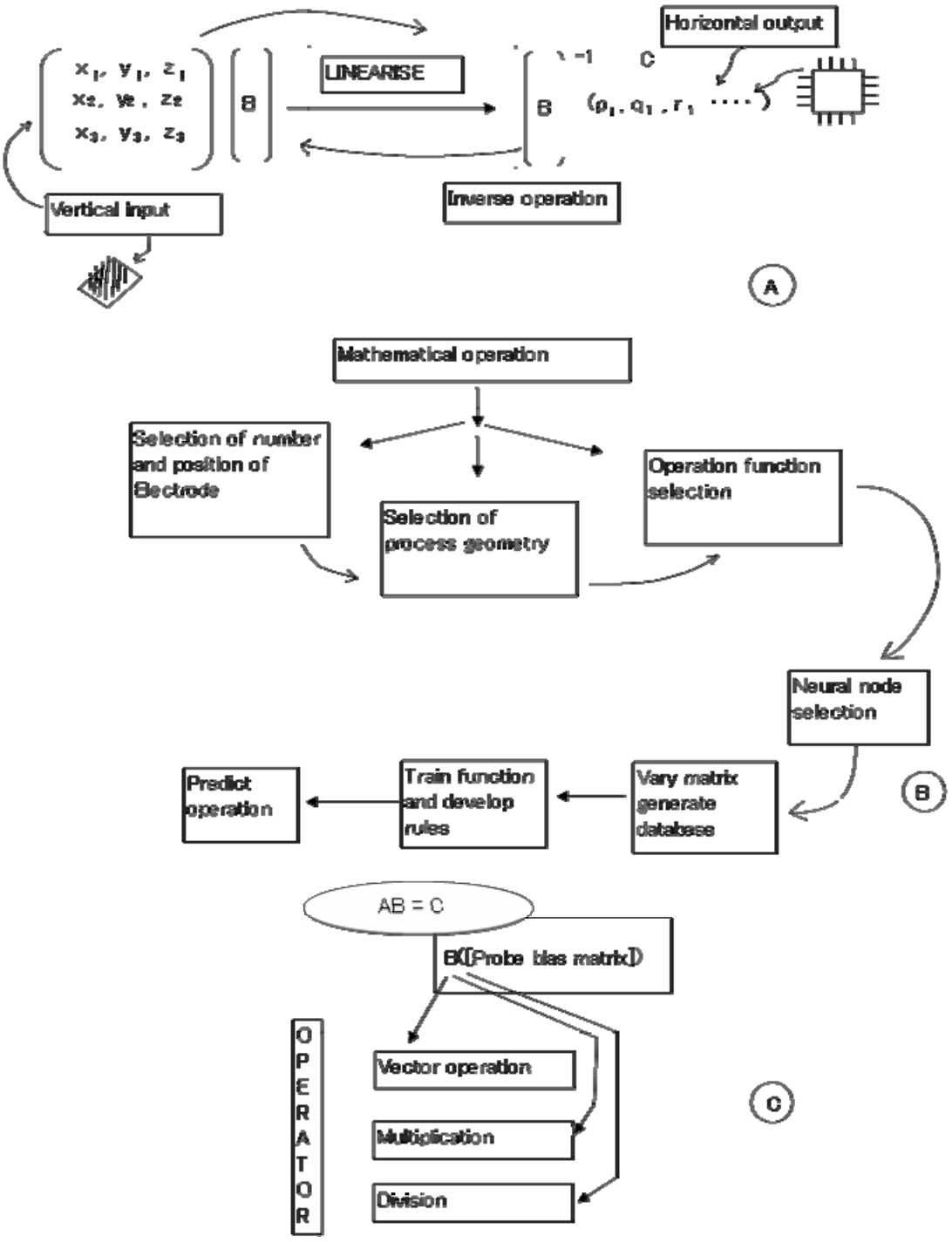


Fig16
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
n
E
1614
n

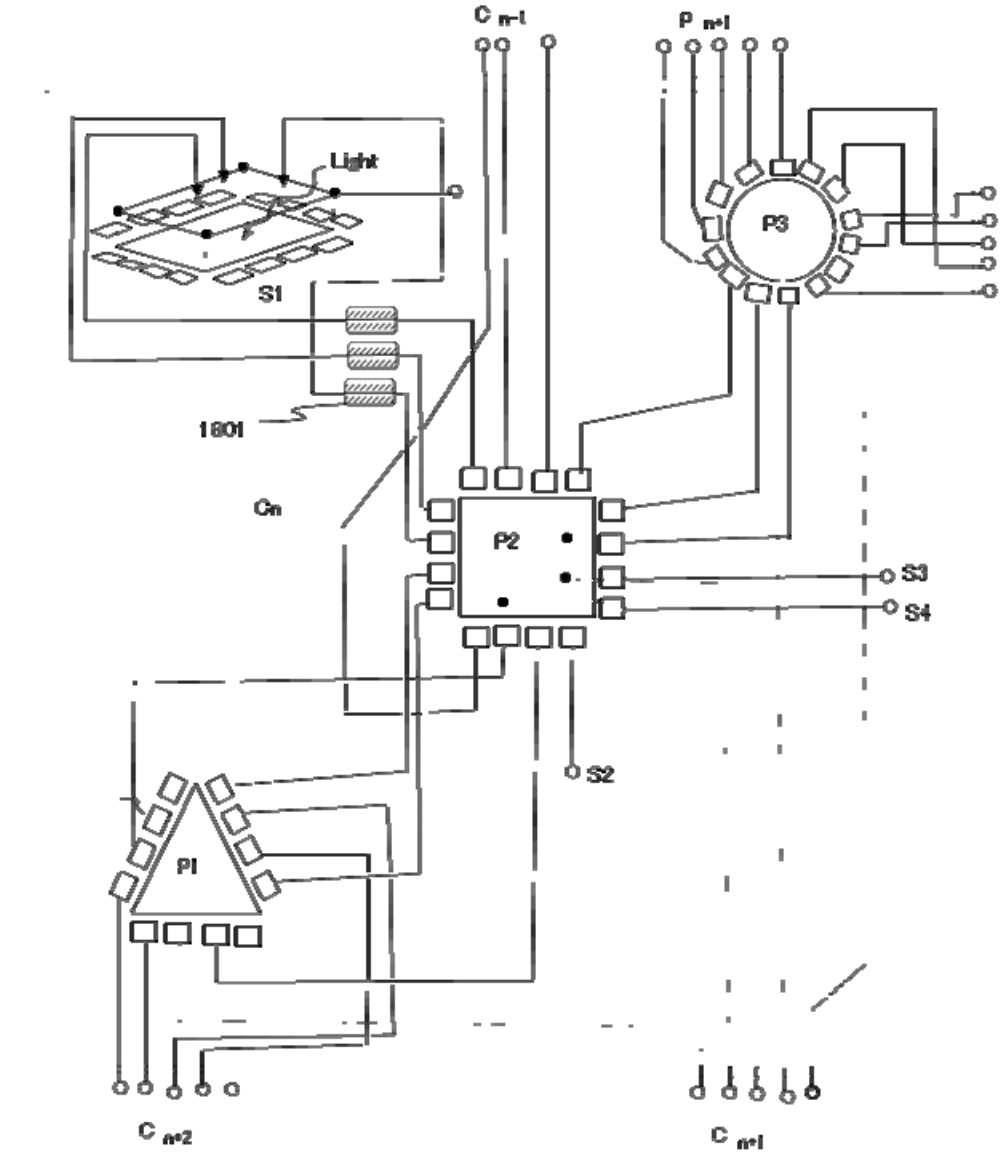
【図１７】

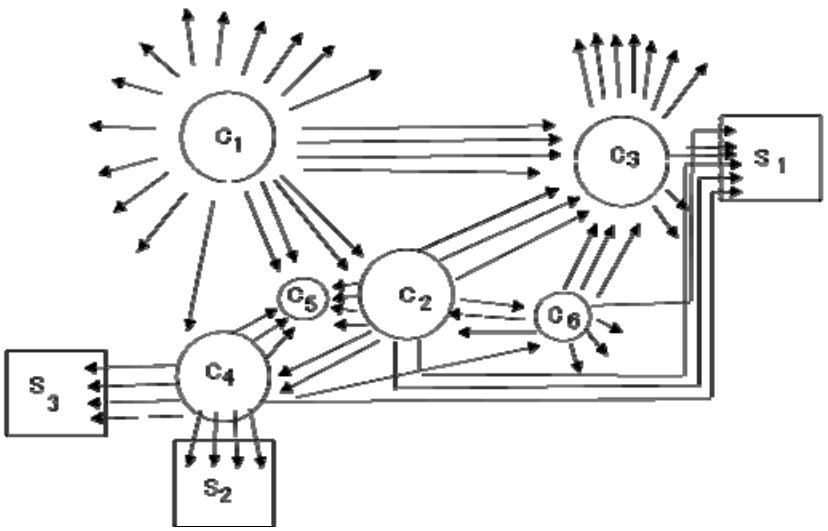
Fig17


Horizontal output
LINEARISE
Inverse operation
Vertical input
A
Mathematical operation
Selection of number and position of Electrode
Selection of process geometry
Operation function selection
Neural node selection
Vary matrix generate database
Train function and develop rules
Predict operation
B
AB = C
B([Probe bias matrix])
OPERATOR
Vector operation
Multiplication
Division
C

【図１８】

Fig18


C n-1
P n+1
Light
S1
P3
1801
Cn
P2
S3
S4
S2
P1
C n+2
C n+1


C1
C3
S 1
C5
C2
C6
S3
C4
S2

【図１９】

Fig19